

**TDA 8046H multi-mode QAM  
demodulator  
Application note  
AN 96048**

### Abstract

*The TDA8046H is a multi-mode QAM demodulator for Digital Video Broadcast applications on cable networks. It generates control voltages for external AGC, Carrier, and Clock recovery control loops. Demodulation to base band I and Q signals is done in the digital domain. A digital half Nyquist filter with a roll-off factor of 15% or 20% satisfies the U.S. and European market requirements. An equaliser reduces the echoes from the channel and is able to convert without training sequence (blind equalisation).*

*For a Hard Decision FEC (Forward Error Correction) interface, a digital output section delivers the symbols in four different formats, two of them including differential decoding. For a Soft Decision FEC interface, the digital output section can be switched to 8 bits wide alternating I and Q data. This mode can also be used to evaluate the behaviour of the constellation before and after equalisation. The output formatter also features a semi-serial output format for FEC interfacing.*

*Due to the I<sup>2</sup>C control interface, a high flexibility is achieved in configuring this chip to adapt to specific application areas. Also the internal status can be read, e.g. lock, S/N estimation, equaliser status.*

*Furthermore, this report contains worked-out examples for applications at a symbol rate of 5 and 6.875 Msymbols per second and contains sufficient theory and simulations to design the TDA8046H in other applications.*



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**Author(s):**

**Robert van Apeldoorn  
Philips Semiconductors - Systems Laboratory Eindhoven,  
The Netherlands**

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## Application note

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### Introduction

The TDA8046H is a widely used integrated multimode demodulator intended for demodulation of digital transmitted Quadrature Amplitude Modulated information.

This report is intended to provide application support for QAM receivers with the TDA8046H integrated circuit. The digital blocks in the TDA8046H are discussed to give the engineer a better understanding how the chip operates. The application note contains methods to optimize loop dimensioning and worked-out examples of commonly used application circuits.

Chapter 1 starts with a general introduction in QAM. Furthermore some important figures of merit, like the commonly used BER v.s. S/N curve are explained. Also basic DVB QAM receiver architecture using the TDA8046H are discussed.

Chapter 2 describes the functional blocks of the TDA8046 and their use to the QAM demodulator. It contains information about digital Half Nyquist filtering, Intersymbol Interference, equaliser, etc.

Chapter 3 methods how to implement the TDA8046H in a specific application are given with respect to the analogue and digital loops in the front-end architecture.

Chapter 4 is a description of the OM5701 application board. All the functions of this board will be discussed. And detailed application information is given by the board schematics.

Chapter 5 introduces the reader in methods to how measurements can be done on the OM5701 application board. It also contains some actual measurements done on the application board.

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## 1. General

The TDA8046H is a single chip QAM demodulator for Digital Video Broadcast applications via cable transmission. Symbol rates up to 7 Msymbols per second can be received. For 256 QAM, the system is capable to achieve lock for low signal to noise ratio's ( $S/N > 27$  dB). For 64, 32, 16 and 4 QAM the lowest S/N's are 21, 18, 15, and 9 dB respectively.

To demonstrate the functionality, an application board called the OM5701 has been developed. This board and the measurement methods are also described in this note.

As the demodulation is done in the digital domain, The analogue signal is sampled at symbol frequency. An external 8 bits AD converter (TDA8714) is sufficient for the 64, 32, 16 and 4 QAM mode. For 256 QAM, a 9 bits AD converter (TDA8761) is required.

The TDA8046H performs digital demodulation to base band I and Q signals, Half Nyquist filtering, equalisation and de-mapping.

Control signals are generated for the external crystal oscillator for the symbol clock, carrier oscillator and AGC.

On board DAC's convert the digital loop outputs to analogue currents which are applied to on board OPAMP's with external feedback loops containing integrating components. The dimensioning of these loop filters is done with resistors and capacitors.

With I<sup>2</sup>C the system behaviour can be adapted by software if required to changing conditions.

### 1.1 Quadrature Amplitude Modulation

For QAM modulation two amplitude modulated carriers, an I and a Q carrier, are multiplied with a phase difference of 90 degrees. This is done with the help of a complex multiplier. A schematic diagram of a complex multiplier is given in Fig.1.

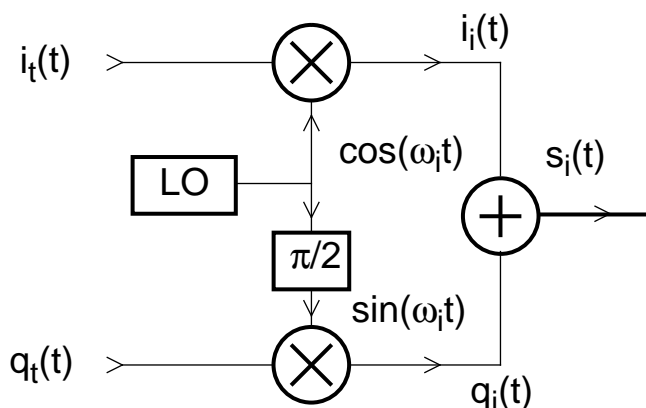


Fig.1 Complex multiplier

The number of steps in which the I (in phase) and Q (quadrature) carriers can be amplitude modulated determine the number of constellation points.

A constellation diagram consists of an array of constellation points. This is shown in figure Fig.2. A constellation point consists of samples of  $S_I(t)$  at fixed time intervals where the information is considered valid. This samples can be translated to certain positions on an I axis and certain positions on Q axis. The phase difference is represented in the orthogonal relation of the I and Q axis.

When I and Q can be modulated in N=six discrete steps, the number of constellation points (M) that can occur is:  $M=2^N$  or  $M=64$  QAM.

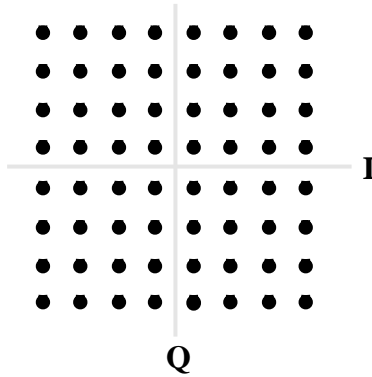


Fig.2 64QAM constellation diagram

The general form of M-ary QAM is defined by the transmitted signal (NB: Nyquist filtering is disregarded here):

$$s_i(t) = \sqrt{\frac{2E_o}{T_s}} a_i \cos(2\pi f_c t) + \sqrt{\frac{2E_o}{T_s}} b_i \sin(2\pi f_c t) \quad \text{for } 0 \leq t < T_s \tag{1}$$

where  $E_o$  is the energy of the signal with the lowest amplitude, and  $a_i$  and  $b_i$  are a pair of independent integers chosen in accordance with the location of the message points. They can be chosen in the range -7, -5, -3, -1, 1, 3, 5, 7.

The signal  $s_i(t)$  consists of two carriers in phase quadrature, each of which is modulated by a set of discrete amplitudes; hence the name quadrature amplitude modulation.

The constellation diagram can actually be measured when the I and Q information is available, using a vector analyser. The information coming from such a constellation is very interesting for system design as the position and shape of the constellation points can tell much about the condition of the I and Q signals. In this way system and channel impairments can be made visible.

### 1.2 BER versus S/N curve

The BER (Bit Error Rate) is a number indicating the rate of bits which are erroneous. These errors can be caused by external factors like for example noise or EM pulses added to the signal containing information during transmission of information in digital communication systems. In a constellation diagram these impairments can be observed as an increment of the surface of the constellation points. As the chance of a possible partly overlap increases, the BER will increase.

The performance of a QAM demodulator is usually presented in the form of a BER versus  $E_b/N_0$  graph, as can be seen in figure Fig.3. In this figure, two lines can be seen:

1. A curve which represents the theoretical relation between the BER and the  $E_b/N_0$  ratio in case an ideal QAM demodulator is used.

Theoretically, the BER for a certain  $E_b/N_0$  is depicted by:

$$BER = \frac{4}{\log_2 M} \left( 1 - \frac{1}{\sqrt{M}} \right) Q \left( \sqrt{\frac{3 \log_2 M E_b}{(M-1) N_0}} \right) \tag{2}$$

More information about this relation is given in “Theoretical BER/SER curve” on page 54. A relation between S/N and  $E_b/N_0$  is given in “Relation between  $E_b/N_0$  and S/N” on page 60.



2. The actual relation between  $E_b/N_0$  and BER when a practical QAM demodulator is used.

The difference between these two lines gives an indication of the performance of a practical QAM demodulator. As a figure of merit, the difference between the theoretical and practical performance of a demodulator at a BER of  $1E-4$  is called "IL", which stands for Implementation Loss. This Implementation Loss is widely used in channel demodulation theory and practice.

The BER at which the IL is measured is the point where the BER value just meets the DVB spec for quasi error-free operation. The IL is measured *before* forward error correction is performed (see paragraph 1.3), which means: after QAM demodulation, unless otherwise indicated.

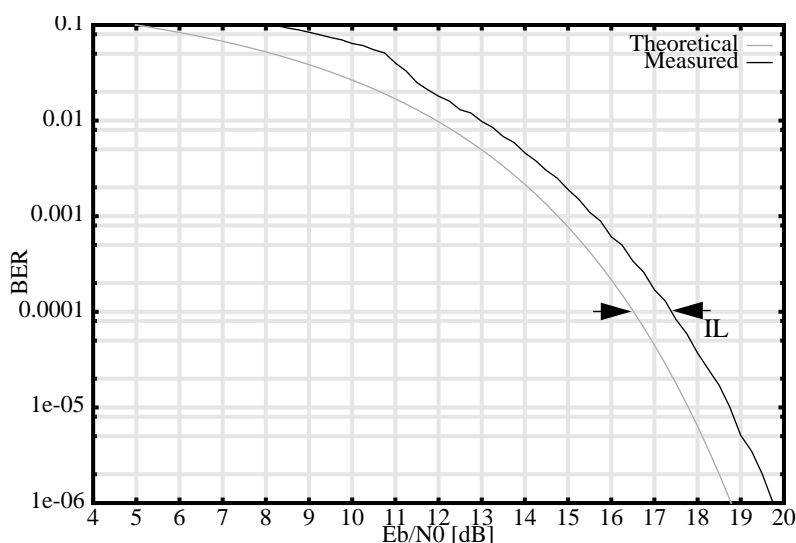


Fig.3 BER measurement for 64 QAM using DVB compliant symbol mapping

*NOTE: All the measurements done in this document are on a indicative base. They can be used for comparison only.*

### 1.3 DVB cable front-end architectures with the TDA 8046H

In Fig.4 an example is given for a typical fixed symbol rate DVB cable front-end.

The input signal is provided by the cable connected to the tuner. This tuner performs down conversion of a selected channel to the IF frequency. The adjacent channels are removed from this spectrum with a SAW filter. The QAM signal on IF is then down converted to the symbol frequency with the help of the IF processing part.

For this HF part of the design several solutions are available:

1. A tuner with a discrete SAW filter and IF processing part (for example the UV916M)
2. An integrated tuner which contains these elements (for example the TD916MK1).

After a channel has been selected and down converted, an LPF filters off the unwanted the mixing products. The remaining baseband QAM spectrum is offered to an analog to digital converter.

The type of ADC depends on the used constellation

- 64 QAM or lower an eight bits ADC is sufficient, for instance the TDA 8790.
- 256 QAM: a nine bits ADC is preferred for example TDA 8761.

The QAM demodulation, AGC detection, carrier recovery and clock recovery as well as output formatting are all covered by the TDA 8046H. This device has a two bits wide data interface to the SAA 7207 FEC decoder as well as an 8 bits data/test interface featuring soft decision FEC output. The SAA 7207 FEC performs hard decision Reed-Solomon Forward Error Correction. The output of this FEC consists of MPEG-2 packets which can be processed by a source decoding solution.

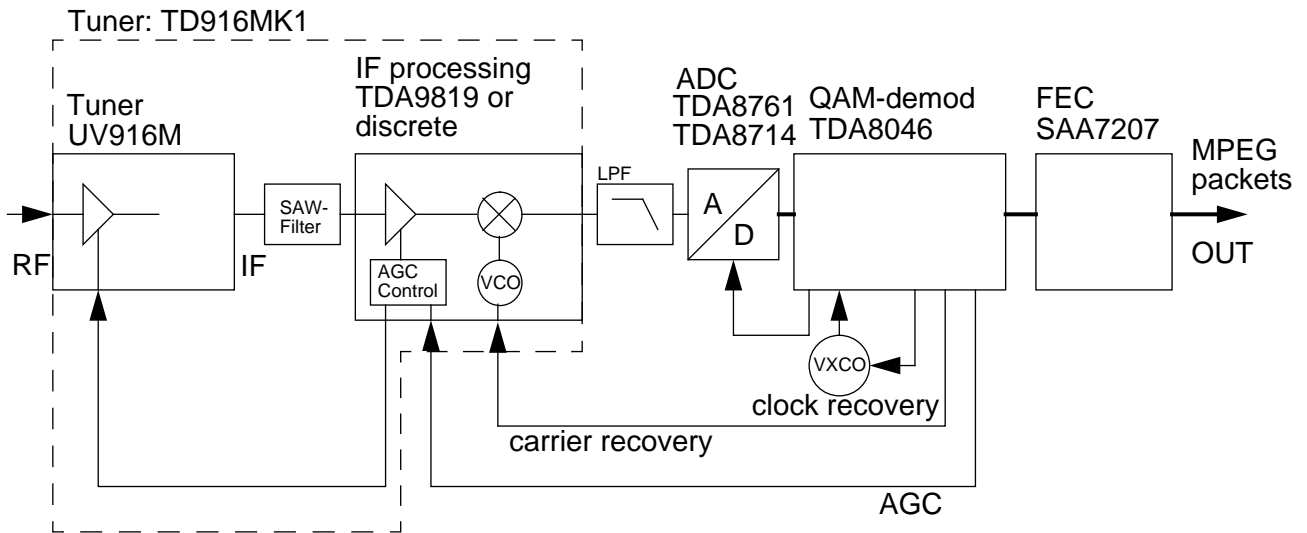


Fig.4 fixed symbol rate cable front-end

The flexibility of QAM demodulation with the TDA 8046H and its external loop structure also enables a variable symbol rate DVB cable front-end solution. An example of this type of cable receiver is given in Fig.5.

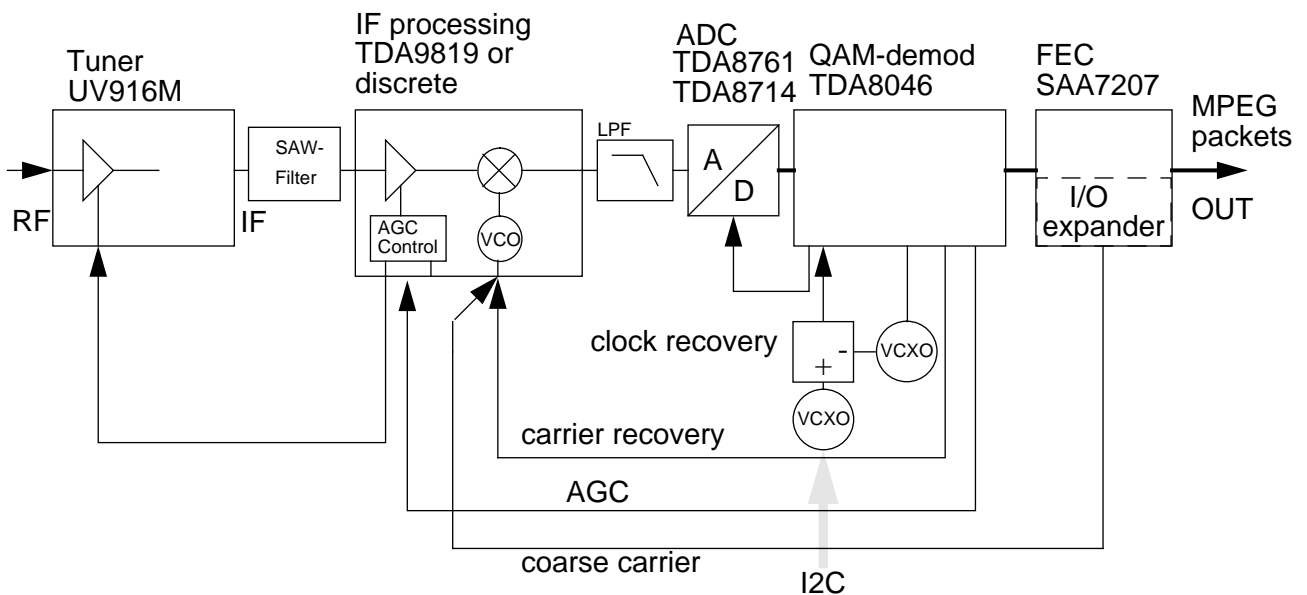


Fig.5 variable symbol rate cable front-end

In the clock loop a programmable synthesizer is added to expand the clock range. The local carrier oscillator range consists of two areas; a coarse one to adapt to the different sample frequencies and a fine one to keep the carrier loop behaviour.

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On the OM5701 application board the discrete IF processing parts, the SAW filter, LPF, ADC and QAM demodulator are available as well as an AGC amplifier to close the AGC loop. To be able to do measurements on the board, a special measurement interface is provided on the board. With this board the TDA8046H QAM demodulator can be evaluated. The board is discussed in more detail in paragraph 4.



## 2. Functional description

The block diagram of the TDA8046H is depicted in Fig.6. The QAM demodulator generates in a digital way the control values for AGC, Carrier Recovery, and Clock Recovery. The on-chip DA converters translate these digital values to analog control currents which are integrated afterwards by an active loop filter. To perform this loop filtering, after each DAC an operational amplifier is implemented.

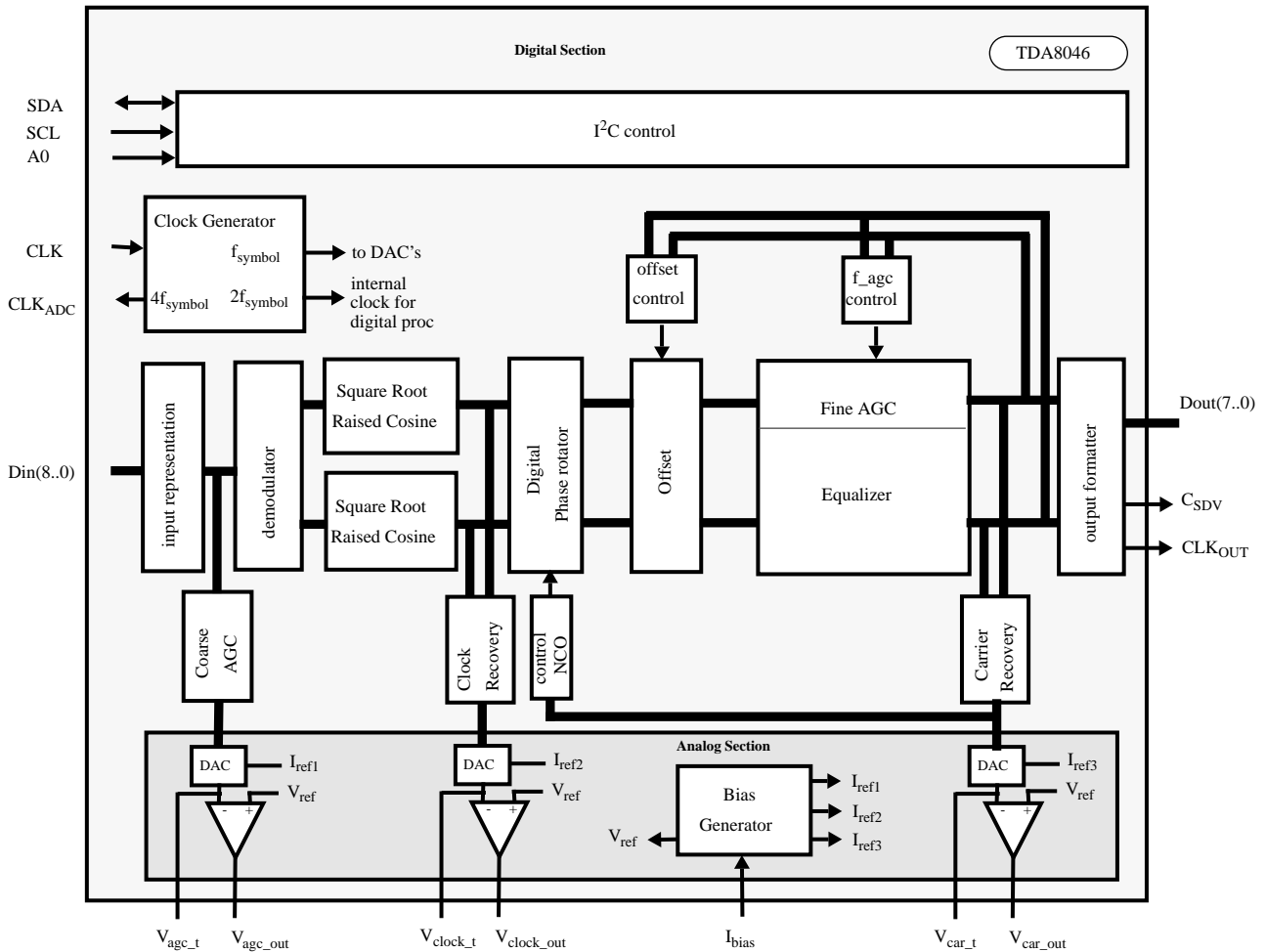


Fig.6 block diagram of the TDA8046H

The carrier recovery consists of a two loop system. The outer loop is shown in the diagram of Fig.12 on page 13 and controls both phase and frequency at a low speed. Due to short feed back path, the inner loop can be operated at a larger bandwidth. This loop is mainly used to reduce the influence of disturbances on the incoming QAM modulated signal. Examples of disturbances are: phase noise and microphonics of the tuner.

Also the AGC consists of two loops; one outer loop called the coarse AGC and one inner loop called the fine AGC. The AGC (see figure Fig.12 on page 23) avoids overloading of the ADC while the fine AGC ensures that the received symbols fit into the constellation template.

The recovered symbols are converted into bits according to a demapping scheme and represented at the output in an 8 bits parallel or 2 bits semi-serial output format. The demodulator can be initialised and monitored by the I<sup>2</sup>C-bus interface.

## 2.1 Input representation

This function selects between 2's complement and straight binary input. The I<sup>2</sup>C switch INP (address="00", D3) selects 2's complement mode when INP=0 and straight binary mode when INP=1.

Under normal conditions, an 8-bits ADC has enough resolution for a 64 QAM or lower transmission schemes. A 9 bits ADC achieves an improvement in implementation loss of 0.1 dB at maximum, especially when adjacent channels are present. Due to the additional power of the adjacent signals, the coarse AGC adjusts the total signal power to the 8 bits window, which results in a reduction of the effective bits for the desired QAM signal. For 256 QAM an 9 bits ADC will give a higher improvement, especially in the case of adjacent channels.

The 8 ADC output bits (7..0) should be connected to the 8 MSB's of the TDA8046H input Din(8..1). To achieve symmetrical input, the LSB input must be connected to the positive supply voltage (Din(0)=1). On the application board the 9 bits TDA8761 is used. On the QAM application board, the ADC runs at 4 times the symbol rate, which is  $4 \cdot 7 = 28$  MHz at maximum.

## 2.2 Demodulator

The demodulation of the input signal to baseband I and Q signals takes place in the digital domain.

As the sampling rate is exactly 4 times  $f_s$ , the cosine and minus sine multiplications are performed by the sequences "+1,0,-1,0" and "0,-1,0,+1" respectively.

This is the default mode and is represented by the I<sup>2</sup>C switch DEM='0' (address="01"; D3). In case DEM='1', these multiplication sequences are "+1,0,-1,0" and "0,+1,0,-1". In this way a high flexibility is achieved for the board design. Suppose there is no frequency spectrum inversion in the channel, the DEM switch should be used as follows

DEM=0

$$f_{\text{car}} = f_{\text{IF}} - f_s \quad (3)$$

DEM=1

$$f_{\text{car}} = f_{\text{IF}} + f_s \quad (4)$$

Note that there is a relation between the DEM switch and the sign of the Phase (Frequency) Detector output current. Changing the sign of the DEM switch implies changing the sign of the PD output of the carrier loop (address "00"; D5) to achieve a stable loop. It may show that when this CARI is not inverted the system stays in lock, but it in a false lock. In this wrong configuration the internal digital phase rotator will try to compensate this 'instable' outer carrier recovery loop, but after some time the whole system will fall out of lock.

## 2.3 Half Nyquist Filters

The filters perform the receiver part of the Nyquist pulse shaping ("half Nyquist filters"). There is one filter in the I and one in the Q branch. Both filters are square root raised cosine, with a Roll Off of  $\alpha=15\%$  or  $20\%$ . The frequency characteristic is shown in Fig.7.

Normal operation is achieved when the I<sup>2</sup>C NYQ switch (address: "00"; D2) stays in the default mode NYQ=1. When NYQ=0 the filters are by passed. This mode is only meant for testing!

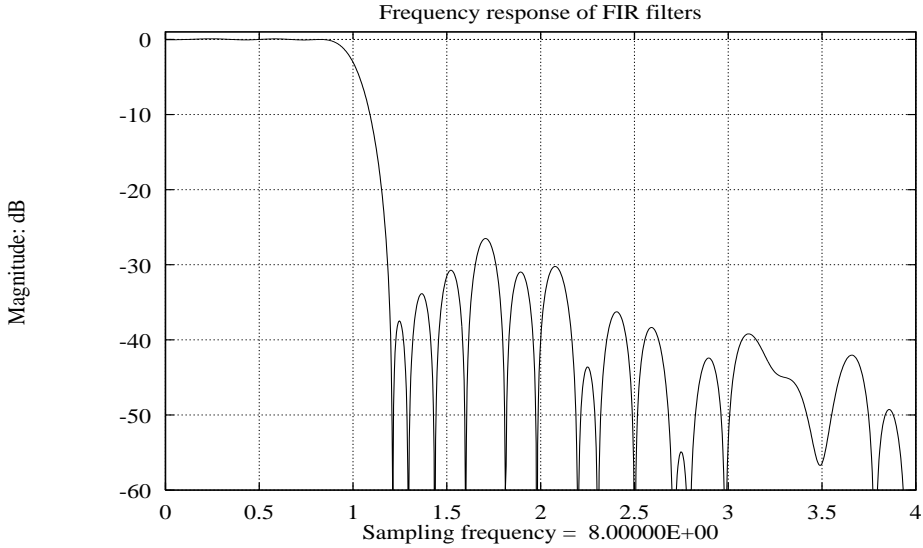


Fig.7 Frequency characteristic of Half Nyquist filter

Due to pulse shaping the Inter Symbol Interference is minimized. It can be expressed in peak amplitude ( $ISI_{peak}$ ) or power ( $ISI_{power}$ ) Inter Symbol Interference. As pulse shaping is partly done in the transmitter and partly in the receiver, the impulse response of the cascaded filters should be analysed. When the coefficients  $h(k)$  represent the impulse response of the cascaded filters (full Nyquist), the peak Inter Symbol Interference is defined as (5)

$$ISI_{peak} = 10^{10} \log \left( \frac{2 \sum_{k=1}^{(K-1)/2} |h(4k)|}{|h(0)|} \right) = -35 \text{ dB}$$

The power Inter Symbol Interference is defined as (6)

$$ISI_{power} = 10^{10} \log \left( \frac{2 \sum_{k=1}^{(K-1)/2} |h(4k)|^2}{|h(0)|^2} \right) = -46 \text{ dB}$$

In words, due to Inter Symbol Interference, each symbol is spread out in time and will disturb neighbouring symbols. Due to the factor 4 oversampling, every 4 sampling moments such a disturbance takes place. So the ratio between the (square of) coefficients  $|h(4k)|$  with  $k=-1, +1, \dots, (K-1)/2$  and (the square of) the midcoefficient  $h(0)$  denotes the  $ISI_{peak}$  ( $ISI_{power}$ ).

The impulse response of the nyquist filters is given in Fig.8

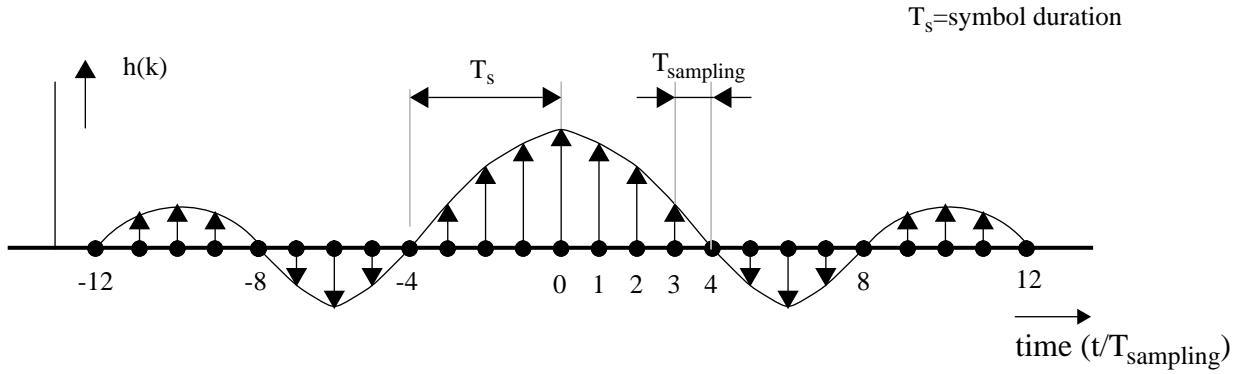


Fig.8 Impulse response  $h(k)=h_t(k)*h_r(k)$

### 2.4 Equaliser

The equaliser performs echo cancellation from  $-5T_s$  (or  $-3T_s$ ) up to  $8T_s$ , where  $T_s$  is the symbol duration. The equaliser type is DFE. The adaptation algorithm is LMS (Least Mean Square). Echoes up to  $8 \times T_{\text{symbol}}$  and pre-echoes up to  $5 \times T_{\text{symbol}}$  can be cancelled.

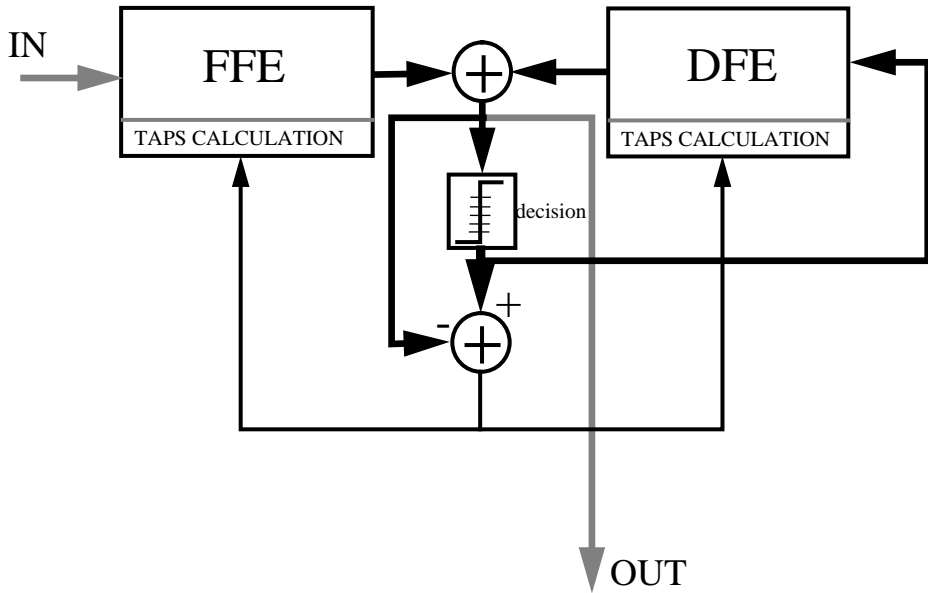


Fig.9 Block diagram of the equaliser

Fig.9 shows the a simplified block diagram of the DFE equaliser in the TDA8046H.



### 2.4.1 Tap diverging

In the application there is a possibility that during acquisition the equaliser is not able to converge, because at that time there may be no QAM signal at all. The taps are controlled in such a way that finally they will diverge to extremes (the tap values rise or fall to a value which is not realistic). When at that time a QAM signal is applied to the QAM demodulator, the signal is too disturbed by the equaliser. Therefore no lock will follow. This can be solved with a preset to the equaliser. There are three possibilities to reset the equalizer:

- Automatic preset of the equaliser

A tap diverging algorithm is implemented generating an ALEQ (Alarm Equaliser) bit. When diverging occurs, the ALEQ bit will be set high. When EAR (Equalizer Alarm Reset) is set high, this ALEQ bit is internally fed back to the reset of the equalizer, resulting in a recovery of the equalizer.

when there is a non-QAM signal (or no signal) applied to the demodulator this process of diverging and resetting will be repeating constantly until a QAM signal is applied. Now the equalizer will converge and the system will be in lock.

This state is default in the OM5701 software. Note that the default value of EAR = 0 so it has to be set after every reset.

- Hardware preset of the complete chip.

PRESET pin 52 to '1' during at least one clock period. As a consequence the whole chip will start from default mode. In case the system is operating NOT in default mode, all settings are restored to default values and have to be set again by I<sup>2</sup>C.

- Software preset of equaliser only

A software PRESET (I<sup>2</sup>C: address 09, D0) only affects the taps of the equaliser. This preset can also be given conditionally. With the help of I<sup>2</sup>C, the lock flag (I<sup>2</sup>C address 03, D0) can be checked. When there is no lock it may be decided to preset the equaliser, or another check can be done which is: check if one of the taps (TDM3, TCM3), (TDM2, TCM2), (TDP7, TDC7), (TDP8, TDC8) are above 87.5% of the maximum. In this case it is sure that it was the equaliser that was diverged and a preset could be applied.

### 2.4.2 False lock

When no signal is applied to the TDA8046H the equalizer may converge to a state where the constellation dots, normally for no input signal all positioned exactly in the centre of the constellation diagram, fall into one or more "count windows" (see paragraph 2.6.2). In this case the lock detector counts a value larger than LDT (lock detector threshold) and the LK (lock) indicator will be high. This is called "false lock". This is a stable condition. It however recovers from this condition when a signal is applied to the TDA8046H

This "false lock" condition can be a problem in a scan/search-application (using a low-noise tuner) where the demodulator searches a certain low-noise band for QAM signals. It can easily be avoided by looking with the software at the LK signal and the DAC AGC 4-bit value. Now a lock signal can be generated only when there is sufficient input power so false lock cannot occur.

### 2.4.3 Equaliser operation modes

The Equaliser is controlled by the I<sup>2</sup>C parameters PRESET, EDFE, EFFE, EFC, EAR, FFEL:

**TABLE 1 Equaliser I<sup>2</sup>C settings**

parameter	bit	value	description
Equalizer	PRESET	0	normal operation
		1	coeff. to zero (main tap to 1)
	EDFE	0	normal operation
		1	freeze coefficients of DFE part
	EFFE	0	normal operation
		1	freeze coefficients of FFE part
	EFC (Fine AGC (Eq. Fr. Centre tap))	0	normal operation
		1	freeze centre tap, no fine agc
	EAR	0	Automatic Reset switched OFF
		1	Automatic Reset switched ON
	FFEL	0	3 taps in FFE part
		1	5 taps in FFE part

TABLE 2 shows the useful combinations of these parameters.

- For combination A, normal operation, all parameters must be '0'.
- For combination B, the coefficients of all taps are set in default mode (main tap '1', rest '0'). The I<sup>2</sup>C parameter PRESET is automatically put to '0' one clock later. This means that NO additional I<sup>2</sup>C action is required to make PRESET='0'.
- For combination C, at a certain moment in time, the taps are frozen. When after acquisition the equaliser taps are 'learned' by the equaliser, they can be frozen. An advantage is that the inherent noise is switched off and that will increase the performance. On the other hand, when the echo profile is changing, it is not adapted by the equaliser.
- For combination D, the equaliser is preset and frozen (in this order). In this way there will be no equalisation action, the equaliser is transparent.
- For combination E the fine AGC is switched off. This is no normal mode and can best never be used. It has been implemented as a test mode to verify the equaliser functionality supposing the gain is correct. But in normal operating conditions, the half Nyquist filter and the equaliser will reduce power which has to be corrected by the fine AGC.

**TABLE 2 Equaliser useful operation modes**

	I <sup>2</sup> C parameters				Equaliser	Fine	Comment
	EFC	EDFE	EFFE	PRESET		AGC	
A	0	0	0	0	on	on	Normal operation
B	0	0	0	1	on	on	Restart normal operation after preset
C	0	1	1	0	off	on	Freeze current tap settings, Echo profile is frozen
D	0	1	1	1	off	on	Freeze default tap settings, Transparent mode
E	1	X	X	X	X	off	Main tap frozen, NO normal operation mode

### 2.4.4 Main tap

The main tap TDC, which is the centre tap of the direct filter, can be set by I<sup>2</sup>C address 0A, D(7..0). In fact there is no reason to set a new value because the fine AGC is a fast loop and is able to correct the TDC value to the desired value within a few hundred symbol periods. This is always faster than forcing the TDC value, because I<sup>2</sup>C is 'slow' with respect to the acquisition time required for fine AGC.

## 2.5 Offset control

When an interference is exactly at the symbol frequency, the constellation diagram will NOT be centred around the origin of the I,Q-plane. Such an offset in the I or Q direction is compensated by the offset control.

In default mode, offset control is switched on (OFFS; I<sup>2</sup>C address 00, D3) when OFFS='1'. When no interference is expected at the symbol rate the offset control may be switched off (OFFS='0'). However, in case of absence of an interfering signal, there is no difference in Implementation Loss when the offset control is switched either on or off. So, best is to switch the offset function on.

## 2.6 Output formatter

This block represents the recovered data in several output formats as given in table TABLE 3. This enables a flexible interface to a FEC unit.

**TABLE 3 Output modes**

I <sup>2</sup> C parameters						output mode	comment
OUTB	OUTA	OUTF	TSEL2	TSEL1	TSEL0		
0	0	0	0	0	0	scheme 1	Differential decoding
0	1	0	0	0	0	scheme 2	Direct translation
1	0	0	0	0	0	scheme 3	Differential dec. Draft prETS 300 429:1994
1	1	0	0	0	0	scheme 4	Direct translation HP8782B/K03
X	X	0	1	1	1	I,Q alternating	I,Q 2's complement output after equalisation: for soft dec. FEC
X	X	0	0	1	1	I,Q alternating	I,Q 2's complement output before equalisation:
X	X	1	X	X	X	semi-serial	for hard dec. FEC (SAA7207)
		rest				test data	Not meant for normal operation

### 2.6.1 Hard decision Error Correction

The schemes 1 to 4 map the I and Q data to symbols. The representation on the output bus d<sub>out</sub>(7..0) is described in the data sheet of the TDA8046 [PHI]. This is a hard representation of the symbols, which only allows hard decision like Reed Solomon decoding.

In the case of OUTF='1', The data stream is converted from an 8 bits parallel to a 2 bits wide semi-serial stream. This format can be used to connect a FEC with 2 bits input (like the SAA 7207) to the TDA8046H.

### 2.6.2 Lock detect

In the output formatter the symbol (built up of I and Q information) is projected on a certain map to translate the symbols in the correct data words. When these symbols are observed over a certain period of time, a constellation diagram is formed consisting of constellation dots.

Around every position where a constellation dot is expected, a certain window is defined. When a symbol falls into one of these windows, a counter is incremented. After a certain number of received samples the counter value is compared to the value of the lock detector threshold LDT. When the counter value is larger or equal to LDT, the lock (LK) bit is set. The interval is determined by the lock detector window size WS.

When for example the dot sizes of the constellation points are too big (due to noise, ISI etc.), many symbols will not fall in the specified window and the counter will have a low value when it is compared to the LDT, resulting in a no-lock indication.

From the counter value also the SER estimation is generated with help of the estimation algorithm. This SER estimation can be read out by the I<sup>2</sup>C bus interface by the Lock detect Estimation byte (LE).

From the SER estimation the S/N ratio of the input signal can be estimated\*).

**Table 4: Lock detector characteristics**

SYMBOL	PARAMETER	min.	typ.	max.	unit	window size	Threshold (LDT)
SNR <sub>lock</sub>	SNR for lock at given constellation format:						
	4-QAM	9			dB	2048	1024
	16-QAM	15			dB	256	98
	32-QAM	18			dB	256	98
	64-QAM	21			dB	256	98

In Table 4: an example is given for window sizes and LDT values for several QAM constellation formats.

\*) In the OM5701 software an S/N estimation is done on the basis of a lookup table getting information from the estimation algorithm. The lookup table for the S/N ratio estimation was based on a theoretical relation in which only ideal white gaussian noise was considered. The number for lock estimation after the demodulator is translated to a number of S/N at the input of the demodulator. When other impairments are responsible for signal degradation (like phase noise, non gaussian noise etc.), this lookup table will no longer be correct. Therefore the reliability of this estimated S/N ratio number is very low. The lookup table used by the OM5701 software is given in “user’s guide for the I2C control program for the TDA8046 demoboard”.

### 2.6.3 Soft decision Error Correction

In case of soft decision error correction interface, the I and Q representation can directly be output to the d<sub>out</sub>(7..0) bus when EQU\_NYQN='1', TSEL='1', TSEL='1' and connected to the FEC. In this output format the I and Q can also be applied to a constellation analyser to investigate the behaviour of the system by means of a constellation diagram. When EQU\_NYQN='0', the I and Q represent the data before equalisation.

symbols		-7	-5	-3	-1	+1	+3	+5	+7									
dout(7..0)	-128	-113	-112	-81	-80	-49	-48	-17	-16	15	16	47	48	79	80	111	112	127

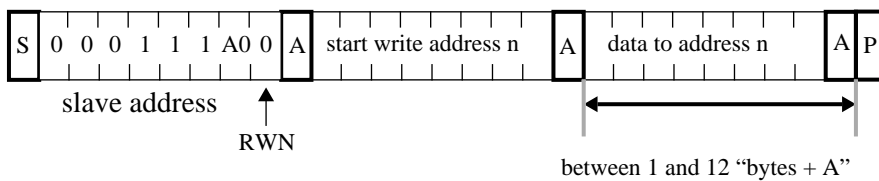
Fig.10 Soft decision interface for I and Q.

Fig.10 shows the I and Q 2’s complement location for the symbols.

## 2.7 I<sup>2</sup>C Control

To achieve a high flexible usage of the TDA8046H, an I<sup>2</sup>C control is implemented. For demonstration purposes and investigation of the TDA8046H, an application board is available. It contains the TDA8046H with an oscillator and a mixer for carrier recovery, a crystal oscillator for clock recovery, a gain amplifier. A measurement interface is based on an Altera EPLD EPM7160 with a serial data output with corresponding clock and analog I and Q outputs for a constellation analyser. Also this EPLD is I<sup>2</sup>C controlled.

### I<sup>2</sup>C Write Protocol



### I<sup>2</sup>C Read Protocol

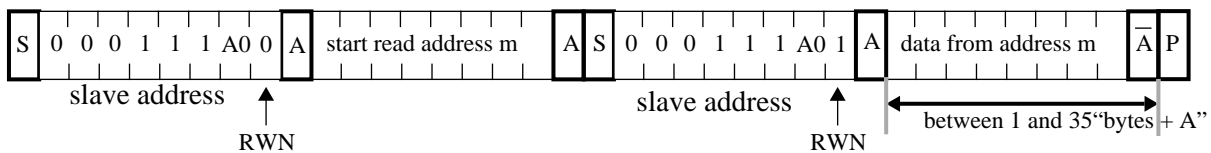


Fig.11 I<sup>2</sup>C protocol to TDA8046H

The control of this board can easily be done with the help of a MENU driven PC program described in the "User's Guide of the I<sup>2</sup>C Control Program for the QAM demodulator TDA8046". Fig.11 describes the TDA8046H I<sup>2</sup>C protocol.

#### EXAMPLE:

Before Data can be read from the TDA 8046H/C1a, a pointer must be set to the register you want to read from. This must be done with a write action. The correct order should be:

- Start the I<sup>2</sup>C transfer
- Address the chip in question (namely the TDA8046H) with the RWN=0
- Address the register in the chip you want to read
- Start the I<sup>2</sup>C transfer
- Address the chip in question (namely the TDA8046H) with the RWN=1
- Read the data back from the register
- Stop the I<sup>2</sup>C transfer

Start - Adr(0xC0) - Adr(0x10) - Start - Adr(0xC1) - Data(0xFF) - stop

also auto increment reads can be done, similar to the write function:

Start - Adr(0xC0) - Adr(0x10) - Start - Adr(0xC1) - Data(0xFF) - Data(0xFF) - Data(0xFF).....etc. - stop



### 3. System loops

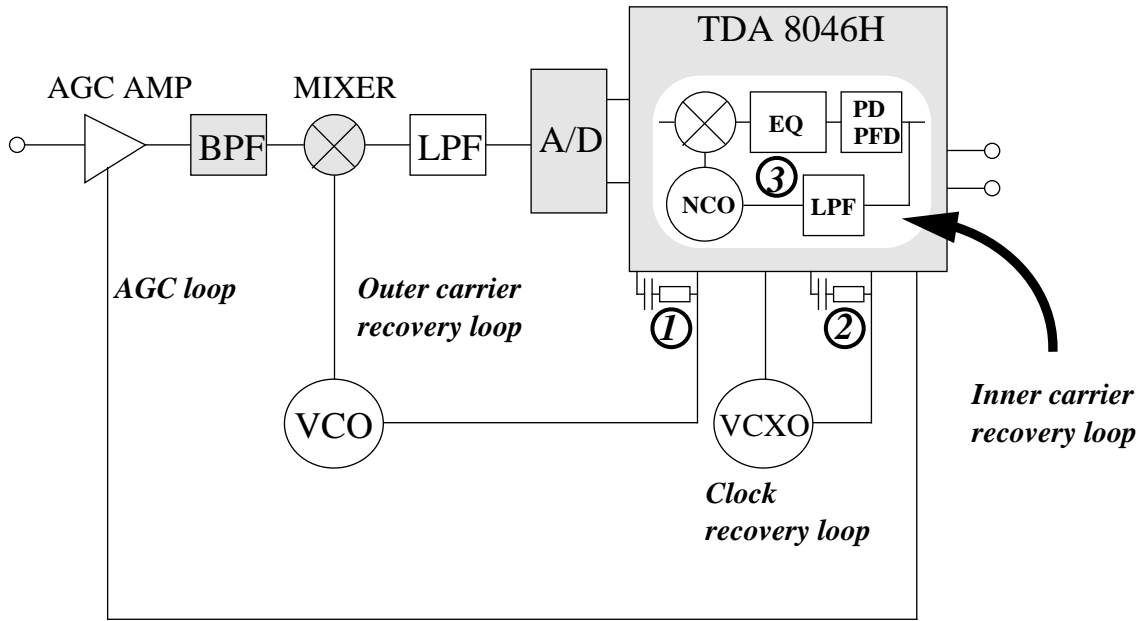


Fig.12 Loops in the QAM demodulation system

For the application of the TDA 8046H loops are required for:

- Carrier recovery (inner and outer loop)
- Clock recovery
- AGC (inner and outer loop)

#### 3.1 Basic system loop structure

For the type of loop used in the TDA8046H basic application, the following relation between the Bandwidth and the natural frequency exists during acquisition of a loop:

$$2 \cdot \Delta\omega_L = \Delta\omega_{(-3dB)} = B \quad \text{for} \quad \zeta = 0.7 \tag{7}$$

The lock-in range is determined by:

$$\Delta\omega_L = 2 \cdot \zeta \cdot \omega_n \tag{8}$$

To be able to achieve fast acquisition, the lock-in range must be larger than or equal to the VCO range seen at fs:

$$2 \cdot \zeta \cdot \omega_n \geq \Delta f_s \quad \text{or} \quad 2 \cdot \zeta \cdot \omega_n \geq \frac{\Delta f_{VCXO}}{4} \tag{9}$$

When the VCO range is larger than the lock-in range, the loop may require relative more time to acquire lock as the VCO sometimes has to be “pulled in” the lock-in range. This depends on the frequency of the VCO at the begin of acquisition.

This can also be seen in Fig.13 where the start frequency of  $f_{VCO1}$  will almost immediately cause lock, and the start frequency  $f_{VCO2}$  must be pulled into lock resulting in a longer acquisition time.

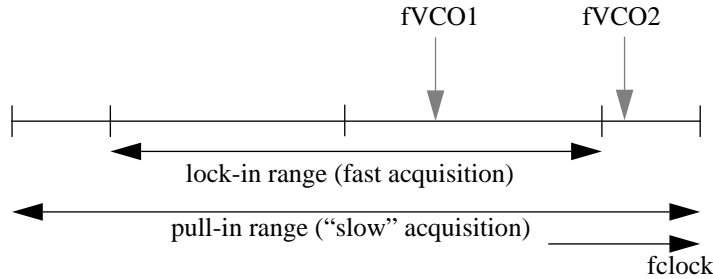


Fig.13 The VCO frequency at the start of the acquisition will cause different acquisition times

In general it can therefore be said that to require a fast lock:

- The natural frequency of a loop should be high enough.
- The frequency range of a VCO should not be too large.

### 3.2 Clock recovery

This function synchronizes the system clock to the rate of the incoming symbols. The clock recovery algorithm maximizes the energy with respect to the sampling moment.

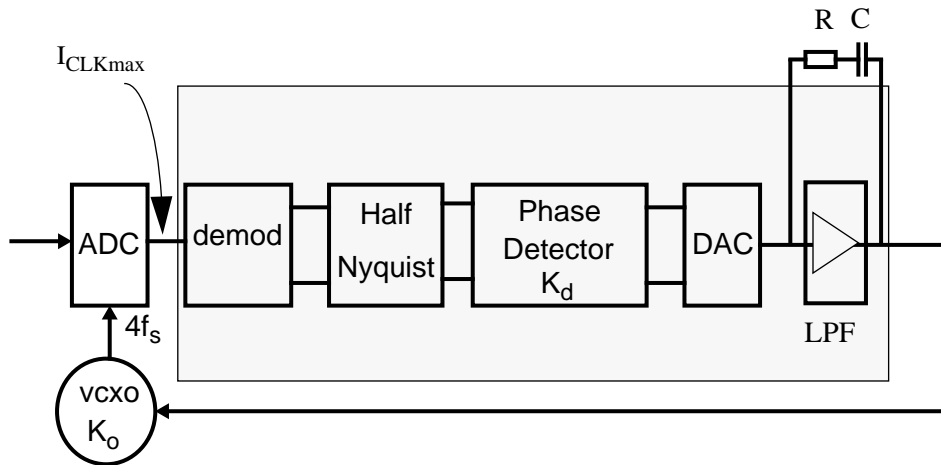


Fig.14 Block diagram of Clock Recovery Loop

The Clock Recovery loop is depicted in Fig.14. The ADC is running at  $4 f_s$  and controlled by an external crystal oscillator with constant  $K_o$ . The Half Nyquist filter is part of the loop, because the clock can best be recovered when the ISI has been reduced. Therefore, the phase detector, with constant  $K_d$ , is placed after this filter. The loop filter is of type Low Pass (LPF, working as an integrator) and is implemented with the help of an OPAMP. The dimensioning of this second order loop is determined by an external resistor  $R$  and an external capacitor  $C$  connected between the OPAMP output and inverting input.

With the help of the  $I^2C$  controlled switches CLKI, CLKB, and CLKA,  $I_{CLKMAX}$  can be changed and thus  $K_d$  (see TABLE 5). CLKI inverts the sign, while CLKB and CLKA control  $|I_{CLKMAX}|$ .



K<sub>d</sub> is determined for the worst case S/N conditions for 256, 64, 32, 16, and 4 QAM which are 27, 21, 18, 15, and 9 dB respectively, and is independent of the QAM mode. For higher S/N, K<sub>d</sub> will be slightly higher (up to ≈ 20%).

**TABLE 5 Clock Recovery Phase Detector K<sub>d</sub>**

NR	I2C Control parameters			Phase Detector	
	CLKI	CLKB	CLKA	I <sub>CLKMAX</sub> [μA]	K <sub>d</sub> [μA/rad]
1	0	0	0	50	12.0
2 (Default)	0	0	1	100	24.0
3	0	1	0	150	36.0
4	0	1	1	200	48.0
5	1	0	0	-50	-12.0
6	1	0	1	-100	-24.0
7	1	1	0	-150	-36.0
8	1	1	1	-200	-48.0

### 3.2.1 Calculation of the loop components

The current I<sub>CLK</sub> is filtered by an LPF, implemented with an OPAMP with the external components R and C. The R and C values can be described as:

$$C = -\frac{K_o K_d}{4\pi^2 f_n^2 N} \tag{10}$$

$$R = -\frac{4\pi f_n N \zeta}{K_o K_d} \tag{11}$$

Where K<sub>o</sub> denotes the oscillator constant in rad/Vs and N denotes the oversampling factor. The clock oscillator is running at 4 f<sub>s</sub>, which gives N = 4. On the application board, K<sub>o</sub> has a negative sign (varicap connected to V<sub>dd</sub>) to compensate for the inverting LPF. Another possibility is to connect the varicap to V<sub>ss</sub>, but this requires an I<sup>2</sup>C setting (NR4, 5, 6, or 7) other than the default one (see TABLE 5).

The equation for the natural frequency (f<sub>n</sub> = ω<sub>n</sub>/2π) and the damping ζ equals

$$f_n = \frac{1}{2\pi} \sqrt{\frac{-K_o K_d}{NC}} \tag{12}$$

$$\zeta = \pi f_n RC \tag{13}$$

### 3.2.2 Dimensioning the loop for optimal in-lock behaviour

The maximum frequency for stable operation is  $f_n < 0.008 f_s$  which implies a maximum natural frequency for stable clock loop behaviour of 40 kHz for the USA and 55 kHz for the EUR application.

A rule of thumb for clock recovery is that the natural frequency must be around  $f_n = \frac{1}{10000} \cdot f_s$ . From simulation it was found that the optimum is around  $f_n=400$  Hz which is always stable.

For a damping of  $\zeta=0.9^{1)}$  and equations (10) to (13), TABLE 6 gives the values for R,C and  $f_n$  found for this optimum:

**TABLE 6 Clock recovery loop parameters**

<b>Fs</b>	<b>fn</b>	<b>R</b>	<b>C</b>
USA (5 MHz)	410.7 Hz	180 k $\Omega$	3.9 nF
EUR (6.875 MHz)	403.2 Hz	120 k $\Omega$	4.7 nF

1) Note that for 5 Msymbols/sec the damping is chosen at 0.9. This is an arbitrary choice. A damping of 0.7 may have an advantage when the propagation delay in the loop becomes critical with respect to the natural frequency. But for  $f_n=400$  Hz it makes no difference (see carrier recovery).

### 3.2.3 Dimensioning the loop for optimal acquisition behaviour

For fast acquisition at a  $f_n$  of 400 Hz and a  $\zeta$  of 0.9 the lock-in range becomes:

$\Delta\omega_L = 2 \cdot \zeta \cdot \omega_n = 4.5 \frac{\text{krad}}{\text{s}}$ . The VCXO runs at  $4 \times f_s$  so the  $\Delta\omega_{\text{VCXO}}$  becomes  $18 \frac{\text{krad}}{\text{s}}$ . or  $\Delta f_{\text{VCXO}} = 2.87$  kHz for the lock-in range.

The pull-in range is limited by the VCXO tuning range which for the OM5701 board is 3.1 kHz for the US standard and 3.6 kHz for the EUR standard.

As the lock-in range is covering most of the pull-in range, the acquisition time of this loop is relatively short. Therefore optimization will be most profitable in the in-lock behaviour.

### 3.2.4 Relation of the clock recovery loop to the carrier offset

First, the clock has to lock onto a QAM signal before the carrier recovery loop can lock. Therefore, the carrier oscillator frequency, which before lock has a certain offset, must lie within a certain range from the actual carrier frequency to enable clock lock. This maximal range is around +/- 600 kHz (measured at  $f_s=6.875$  MHz).

The range in which the clock can lock onto the QAM signal must be larger than the range of the carrier recovery oscillator to guarantee successful acquisition.

### 3.3 Carrier recovery

The carrier recovery loop basically performs two tasks:

1. Acquisition of the signal carrier frequency and tracking it
2. Minimizing the effect of phase noise and microphonics

The combination of a good phase noise cancelling behaviour and a good recovery from microphonics on one hand, and loop stability requirements limited by the propagation delay on the other, requires a double loop structure as can be seen in Fig.15.

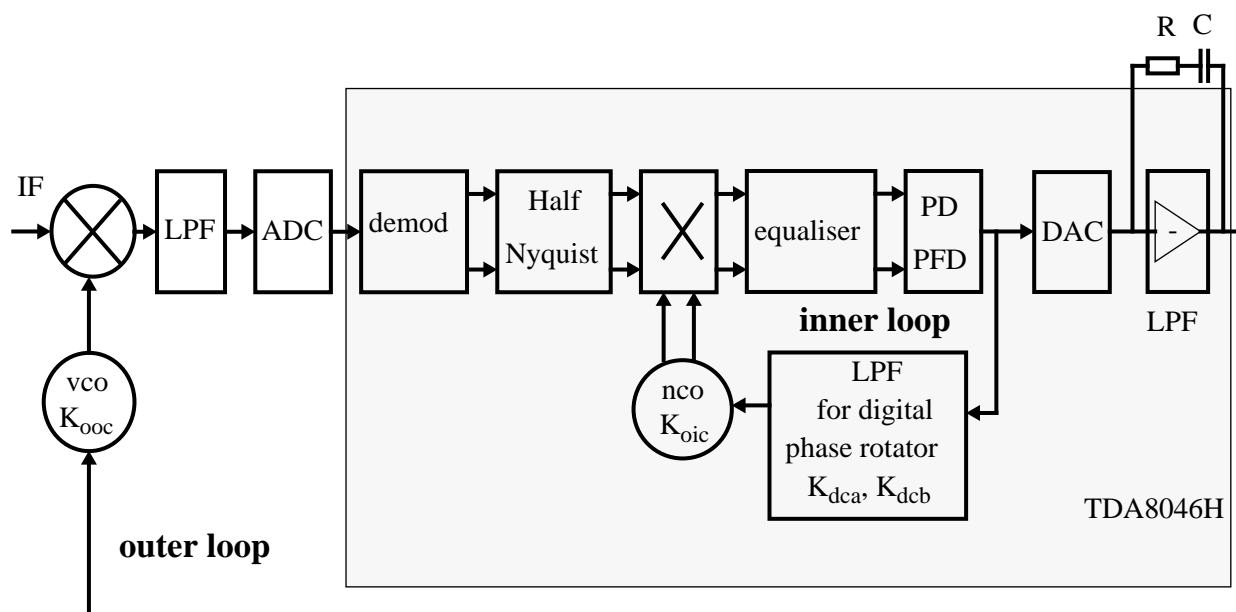


Fig.15 Block diagram of Carrier Recovery Loops

The outer loop controls phase and frequency. Frequency errors are adjusted by an automatic frequency control (AFC) unit implemented in the phase / frequency detector (PD/PFD). As long as the TDA8046H is unlocked, the detector will function as a PFD. When lock is reached, the detector automatically switches to normal PD.

As a result of the outer loop carrier recovery, the incoming QAM signal at the IF frequency is positioned optimal for the demodulation to baseband and for pulse shaping (Half Nyquist Filtering).

Due to the propagation delay, the loop bandwidth of the outer carrier loop can not be higher than approximately 10 kHz. This bandwidth can be influenced by changing the loop components consisting of an external R and C.

The inner loop controls phase only. Because the propagation delay in this loop is smaller than the outer loop, the loop bandwidth can be larger. Therefore phase noise and microphonics can best be controlled with the inner carrier loop i.s.o. the outer carrier loop. The bandwidth of the inner carrier loop can be influenced by changing the digital loop constants  $K_{DCA}$  and  $K_{DCB}$  by means of I<sup>2</sup>C.

### 3.3.1 The inner carrier loop

When a good behaviour on phase noise and microphonics is required, the natural frequency should be chosen high in order to follow the fast change of the constellation phase. This can be seen in Fig.16.

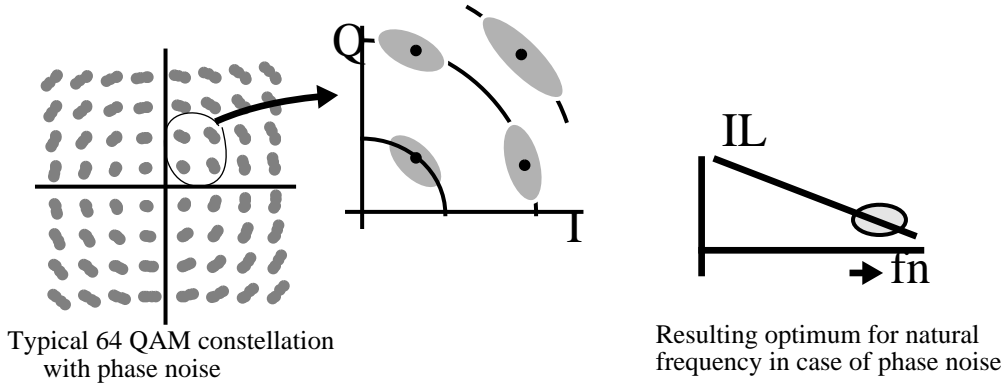


Fig.16 Phase noise behaviour optimization

In order to prevent extra IL due to the loop trying to follow AWGN however, the natural frequency of the inner carrier recovery loop should be chosen low. This is shown in Fig.17.

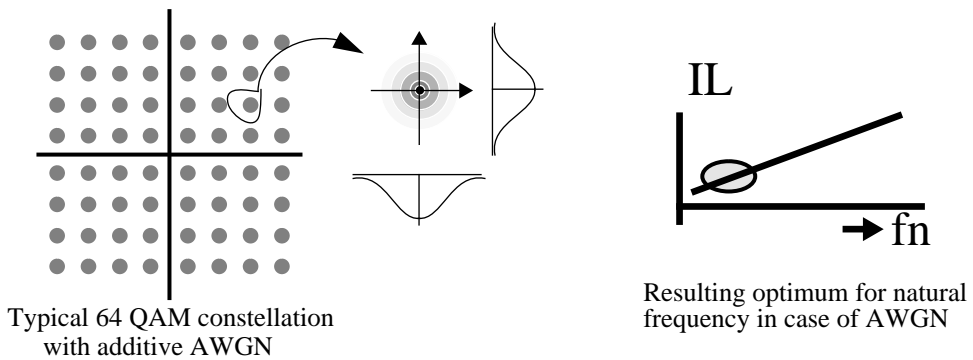


Fig.17 AWGN behaviour optimization

Therefore an optimum must be found between phase noise and AWGN behaviour as can be seen in Fig.18.

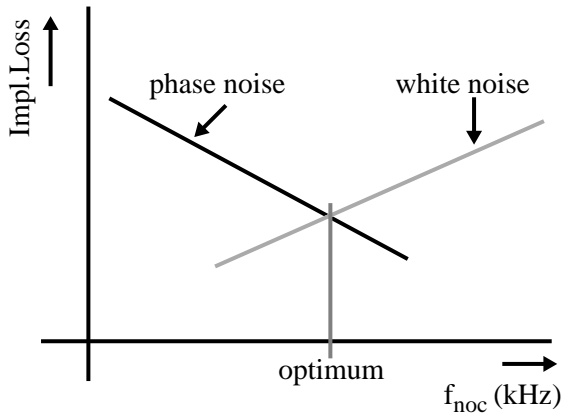


Fig.18 Resulting optimum for the natural frequency in case of AWGN and phase noise

### **Calculation of the loop components**

The inner loop is a second order loop and consists of a Phase Detector with constant  $K_{pd}$  (see Fig.20), loop filter (proportional and integral) and a numerical controlled oscillator (NCO). The loop filter contains two constants  $K_{dca}$  and  $K_{dcb}$ .

The parameters  $K_{dca}$  and  $K_{dcb}$  are obtained by substituting the desired symbol frequency ( $f_s=1/T_s$ ), the damping factor  $\zeta_{ic}$  and the natural frequency  $f_{nic}$  in equations (14) and (15).

$$K_{dca} = \frac{\zeta_{ic}}{\pi f_n T_s} \quad (14)$$

$$K_{dcb} = \log_2 \left( \frac{K_{dic}}{\pi^2 f_n^2 T_s^2} \right) - 16 \quad (15)$$

The damping can best be chosen equal to  $\zeta_{ic} = 0.707$  at the worst case  $S/N = 21\text{dB}$  for 64 QAM.

A damping factor  $\zeta_{ic} \ll 0.707$  will cause instable response by definition, while a damping  $\zeta_{ic} \gg 0.707$  will cause instability because of the propagation delay in the loop. The natural frequency  $f_{nic}$  is the remaining parameter which depends on the disturbances in the system. For low frequency disturbances a low loop bandwidth is sufficient, while for high frequency disturbances a high loop bandwidth is required to be able to eliminate the disturbances.

Table TABLE 7 shows for 6 different combinations of the loop parameters  $K_{dca}$  and  $K_{dcb}$  at  $S/N = 21\text{dB}$ . For  $K_{dca} = 38$  and  $K_{dcb} = 0$  a high loop bandwidth is achieved ( $f_{3dB} = 58.4\text{ kHz}$ ). High frequency disturbances up to 58.4 kHz are within the bandwidth of the PLL and will be corrected. In addition, the system is more sensitive to white Gaussian noise which is deteriorating the overall system behaviour. For  $K_{dca} = 216$  and  $K_{dcb} = 5$  the loop bandwidth is much smaller ( $f_{3dB} = 10.4\text{kHz}$ ), so the system is not much sensitive for white Gaussian noise any more, but will have a poor response on disturbances with high frequency components. A trade off has to be made between the Implementation Loss IL and the ability to correct disturbances like phase noise and microphonics.

**TABLE 7 Parameters for Inner Carrier Recovery loop 5 Msymbols/sec(64 QAM at 21 dB)**

Combination	$K_{dca}$	$K_{dcb}$	$\zeta_{ic}$	$f_{nic}$ (kHz)	$f_{3dB}$ (kHz)	Comment
1	216	0	0.707	5.2	10.4	Low IL, bad perf. ph. noise.
2	154	1	0.707	7.3	14.6	
3	109	2	0.707	10.3	20.6	
4	78	3	0.707	14.6	29.2	
5	54	4	0.707	20.6	41.2	
6	38	5	0.707	29.2	58.4	High IL, good perf. ph. noise

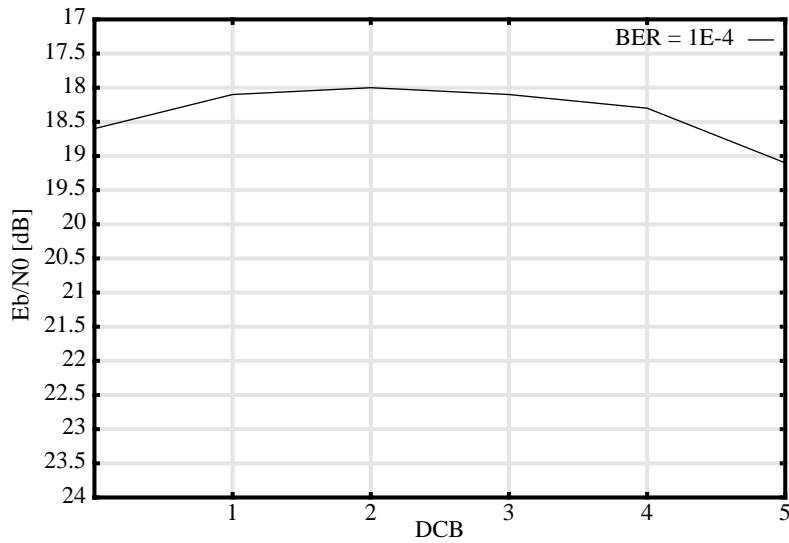
NOTES:

- The maximum natural frequency for stable operation is approximately 30 kHz at a  $S/N$  of 21dB for  $F_s=5\text{MHz}$ .
- For correct loop dimensioning, one should be aware of a phenomenon which is called “threshold extension”; for increasing  $S/N$  ratio the  $f_{nic}$  and thus  $f_{3dB}$  will increase.

### **Dimensioning the loop for optimal in-lock behaviour**

In Fig.18 it could be seen that a certain optimum exists for the dimensioning of the inner carrier loop. The following procedure can be followed to find the correct dimensioning for this loop:

1. As the phase noise is introduced mostly in the applied tuner, first the expected phase noise must be known from this device.
2. Inject the expected tuner phase noise into the system and vary the natural frequency by varying the DCB value with  $I^2C$ . For the correct damping, the value for DCA has to be corrected for each DCB value with the help of formulas (14) and (15).
3. For every DCA and DCB setting, a new BER measurement can be done to determine the maximal allowed  $E_b/N_0$  for a BER of  $1E-4$ . From this information, a graphic can be made like the one in Fig.19.



<b>DCB</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>
DCA ( $\zeta=0.7$ )	160	113	80	57	40	26
Fn [kHz]	7.3	9.9	14	20	28	44

Fig.19  $E_b/N_0$  as a function of DCB values for tuner with  $-96\text{dBc/Hz}@100\text{kHz}$  phase noise

4. From this graphic, the optimum setting can be found. In this optimum the tolerated additional noise is maximum. In Fig.19 the optimum is found for DCB=2. The natural frequency(Fn) for these values of DCA and DCB is 14kHz.

**NOTE:**

During this optimizing, the outer carrier loop should not compensate any phase noise so the natural frequency of this loop should stay low.

in TABLE 8 the optimum bandwidth of for different amounts of phase noise is measured for the OM5701 board

**TABLE 8 Optimal DCB and DCA values for USA**

Phase noise dBc/Hz	DCB	DCA	B (kHz)
-92	3	50	42
-94	3	55	42
-96	2	80	28
-98	2	83	27
-100	1	118	19
-103	1	118	19
< -103	1	123	18.2

For the application board almost no phase noise has to be compensated as it does not contain a tuner. Therefore the inner carrier recovery loop is switched off by default (I<sup>2</sup>C: DPHR=off).

### 3.3.2 The outer carrier loop

The outer carrier loop switches between PD and PFD, PD when there is lock, and PFD when there is no lock. The TDA8046H checks itself whether there is lock. In a certain count window (length=256 for 64 QAM) a counter counts the number of symbols inside a small area around the constellations points. If this number is larger than the threshold value LDT the system is in lock, otherwise the system is not in lock. The LDT value can be controlled by I<sup>2</sup>C. The block diagram can be seen in figure Fig.20.

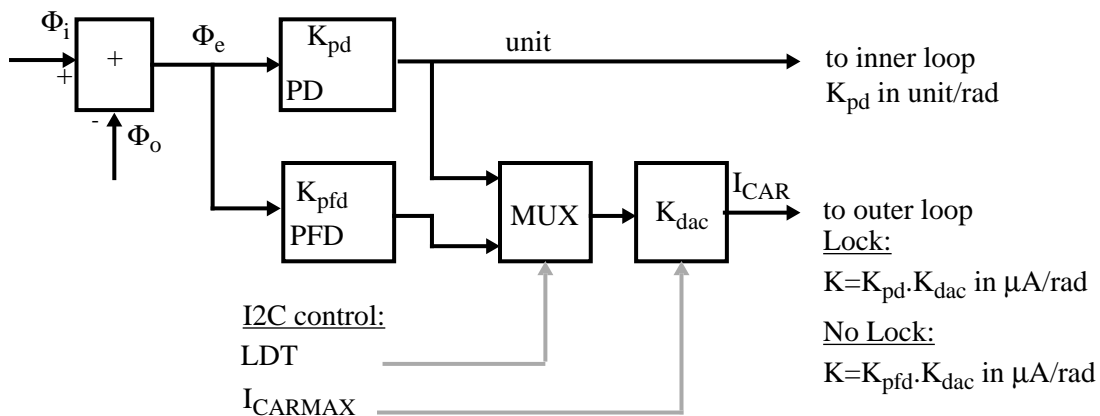


Fig.20 Phase Detector for Carrier Recovery

When the system is unlocked, the phase detector K is a phase / frequency detector. When lock is reached, it is automatically switched to a phase detector. The lock level LDT (I<sup>2</sup>C address 07) can be controlled by means of I<sup>2</sup>C.

The DAC translates the units to a current. The  $K_{dac}$  is dependent on the current  $I_{CARMAX}$  and can be controlled with the  $I^2C$  parameters CARI, CARB, and CARA (see TABLE 9). CARI inverts the current direction, while CARB and CARA determine  $|I_{CARMAX}|$  and thus the gain of K. For cable systems the nominal S/N value equals 30 dB.

**TABLE 9 PD of the carrier loop**

Input control				Phase Detector										PD
$I^2C$			$I_{CARMAX}$ [ $\mu A$ ]	S/N [dB]										Constant
CARI	CARB	CARA		9	14	15	18	21	24	27	30	40	>60	
X	X	X	X	-4.5	-3.2	-3.3	-5	-7	-10	-14	-20	-39	-46	$K_{pd}$ [unit/rad]
0	0	0	50	-113	-80	-82	-125	-175	-250	-350	-500	-975	-1150	
0	0	1	100	-225	-160	-165	-250	-350	-500	-700	-1000	-1950	-2300	
0	1	0	150	-338	-240	-248	-375	-525	-750	-1050	-1500	-2925	-3450	
0	1	1	200	-450	-320	-330	-500	-700	-1000	-1400	-2000	-3900	-4600	K [ $\mu A/rad$ ]
1	0	0	-50	113	80	82	125	175	250	350	500	975	1150	
1	0	1	-100	225	160	165	250	350	500	700	1000	1950	2300	
1	1	0	-150	338	240	248	375	525	750	1050	1500	2925	3450	
1	1	1	-200	450	320	330	500	700	1000	1400	2000	3900	4600	

### Calculation of the loop components

The outer loop is controlled by external R and C values, the  $K_{vco}$  and K. The R and C values can be described as:

$$C = -\frac{K_{vco}K}{4\pi^2 f_n^2} \tag{16}$$

$$R = -\frac{4\pi f_n \zeta}{K_{vco}K} \tag{17}$$

Where  $K_{vco}$  denotes the outer carrier oscillator constant. The equations for the natural frequency ( $f_{noc} = \omega_{noc}/2\pi$ ) and the damping  $\zeta_{oc}$  equal

$$f_n = \frac{1}{2\pi} \sqrt{\frac{-K_{vco}K}{C}} \tag{18}$$

$$\zeta = \pi f_n RC \tag{19}$$

From TABLE 9, we learned that  $|K|$  is small for low S/N.  $f_{noc}$  and  $\zeta_{oc}$  are decreasing when  $|K|$  decreases. For normal operating conditions, the damping may not become too small ( $\zeta > 0.7$ ). This means, that the dimensioning must be done at the worst case conditions. If the S/N improves, the  $|K|$  and thus  $f_n$  and  $\zeta$  increase which influences the loop behaviour positively.



Indeed, when S/N ratio increases, the  $f_n$  is automatically higher and will compensate microphonic distortions better. This is called threshold extension.

### **Dimensioning the loop for optimal in-lock behaviour**

The in-lock phase disturbances are mainly compensated by the inner carrier loop. The main task of the outer carrier loop is therefore restricted to correct frequency offsets which are expected to alternate relatively slow.

To prevent interference with the inner carrier loop behaviour, a safety upper margin of the outer loop natural frequency being 5 times lower than the inner loop natural frequency is advised. This is an approximation.

The maximum frequency for stable operation is 10 kHz at a S/N of 21 dB for the USA standard.

### **Dimensioning the loop for optimal acquisition behaviour**

The acquisition time of this loop is dependent on the several factors:

- The VCO range. A larger VCO range will lead to a larger lock-in range and thus to a longer acquisition time
- Natural frequency of the loop (which is also related to the natural frequency of the inner loop). A higher natural frequency of the outer carrier loop will lead to a larger pull-in range of the loop resulting in a short acquisition time. The restrictions are:
  - The relative long loop delay implies low natural frequencies.
  - The outer loop frequency cannot be too high to prevent interaction with the inner loop.

For the OM5701 application board the outer loop frequency is chosen high enough to give good acquisition behaviour while enabling the inner carrier recovery loop to be switched on. Also a good in-lock behaviour is guaranteed by design the board to remain locked at low S/N ratio's.

For a S/N ratio of 21 dB at 64 QAM and equations (16) to (19) the following values for R, C and  $f_n$  can be found:

**TABLE 10 Carrier recovery loop parameters**

<b>F<sub>s</sub></b>	<b>R</b>	<b>C</b>	<b>f<sub>noc</sub></b>	<b>ζ<sub>oc</sub></b>
USA (5 MHz)	330 kΩ	220 nF	4.2 kHz	1.0
EUR (6.875 MHz)	120 kΩ	4.7 nF	6.0 kHz	0.7

The acquisition and in-lock behaviour must however be optimized depending on the application.

### 3.4 AGC

Fig.21 shows the coarse AGC loop. This loop avoids overloading of the external ADC.

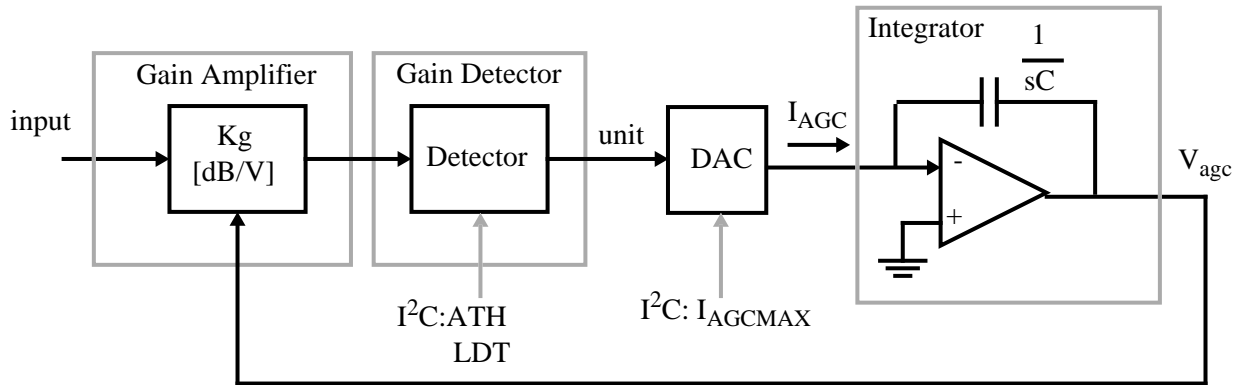


Fig.21 Phase model of AGC Loop

A controllable gain amplifier with constant  $K_g$  (in dB/Volt) amplifies the input signal. A gain detector indicates whether the gain is too high or too low. At 4 times the symbol rate, an average power is calculated and filtered. The coarse AGC adjust the mean power to the AGC Threshold Level (ATH) level, which can be controlled by  $I^2C$ . For each QAM mode, a unique number as indicated in TABLE 11 must be installed by  $I^2C$ . If the system is not in lock, the gain detector generates the code '14' units, while in lock the code '1' unit is generated. The lock status can be adjusted by the LDT threshold

TABLE 11 Coarse AGC threshold levels

Mode	ATH (units)	$I^2C$ data for address 08
4 QAM	496	1F
16 QAM	992	3E
32 QAM	1408	58
64 QAM	1984	7C
256 QAM		

The DAC translates the gain detector output to a current  $I_{AGC}$ . The maximum current and the current direction are controllable with the  $I^2C$  parameters AGCI, AGCB, AGCA, as indicated in TABLE 12. For the TDA8046H application board, the default setting equals  $CARI=0$ ,  $CARB=0$ ,  $CARA=1$ .

TABLE 12 Coarse AGC  $I^2C$  control

$I^2C$ Control			$I_{AGCMAX}$ [ $\mu A$ ]	$I_{AGC}$ [ $\mu A$ ]	
AGCI	AGCB	AGCA		lock	no lock
0	0	0	50	3.6	50
0	0	1	100 (default)	7.1	100
0	1	0	150	10.7	150
0	1	1	200	14.3	200
1	0	0	-50	-3.6	-50
1	0	1	-100	-7.1	-100
1	1	0	-150	-10.7	-150
1	1	1	-200	-14.3	-200

### 3.4.1 Calculation of the loop components

The current  $I_{AGC}$  is integrated by a capacitor across the OPAMP. In the default mode when there is no lock, the capacitor is loaded by a current  $I_{AGCMAX}=100\mu A$ . The delta output voltage  $\Delta V_{AGC}$  in the time interval  $\Delta t$  is described by

$$\frac{\Delta V_{AGC}}{\Delta t} = \frac{I_{AGCMAX}}{C} \tag{20}$$

The gain constant of the whole system  $K_s=\Delta G_{AGC}/\Delta t$  equals

$$K_s = \frac{\Delta G_{AGC}}{\Delta t} = K_g \frac{\Delta V_{AGC}}{\Delta t} = \frac{K_g I_{AGCMAX}}{C} \tag{21}$$

### 3.4.2 Dimensioning the AGC loop

On the application board, the gain amplifier is the BF904, with a gain constant  $K_g=10\text{dB/V}$ . The dynamic range is 30 dB. Now the dimensioning can be done easily. Suppose the dynamic range of  $\Delta G_{AGCMAX}=30\text{ dB}$  must be covered in  $\Delta\tau=1\text{ msec}$ , then with  $K_g=10\text{dB/V}$  and  $I_{AGCMAX}=100\mu A$  the capacitor  $C=32.2\text{ nF}$ :

$$C = \frac{K_g \Delta\tau I_{AGCMAX}}{\Delta G_{AGCMAX}} = 32.2\text{ nF} \tag{22}$$

On the application board 30 nF has been selected.

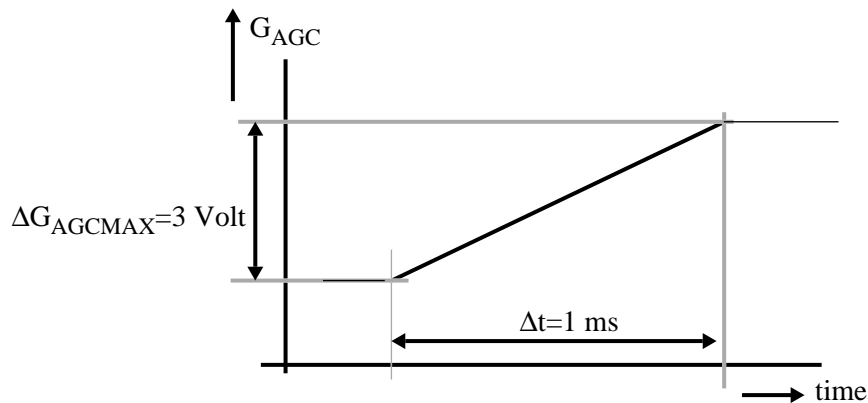


Fig.22 Coarse AGC

The AGC must be a low speed control, so we can fix a low limit at the time constant at 1 ms as depicted in Fig.22. An internal fine AGC in the TDA8046H follows gain offsets in a range of +/- 6dB on a high speed, i.e. 6 dB per 256 symbols at maximum.



## 4. The application board

Schematic 1 shows the different functions on the application board.

The application board can be changed for using a variety of different symbol frequencies and IF-frequencies. At this moment two commonly used IF/symbol frequency sets are supported: A set called USA and a set called EUR. For these sets the difference in component values are shown under the relevant schematics.

This application board has a QAM demodulation section and a measurement interface. The QAM demodulation section contains:

- An IF processing part (schematic 2)
- A base-band processing part (schematic 3)
- The demodulator TDA 8046H (schematic 4)
- An oscillator for generating the clock signal (schematic 5)

### 4.1 The IF processing part

The signal coming from a signal generator must be in the range from -5 dBm to -20 dBm into  $50\ \Omega$ . This signal is led through an AGC stage of which the main function is to close the AGC loop of the QAM demodulator. In a receiver application, the AGC loop will be closed in the tuner or IF processing part.

The AGC can handle input variations on the IF\_input. For correct operation the level can be varied between 87dB $\mu$ V and 102dB $\mu$ V ( $50\ \Omega$ ). Fig.23 shows the transfer characteristic of the AGC measured at a constant output level of 97dB $\mu$ V. This level corresponds with the output level needed on the board.

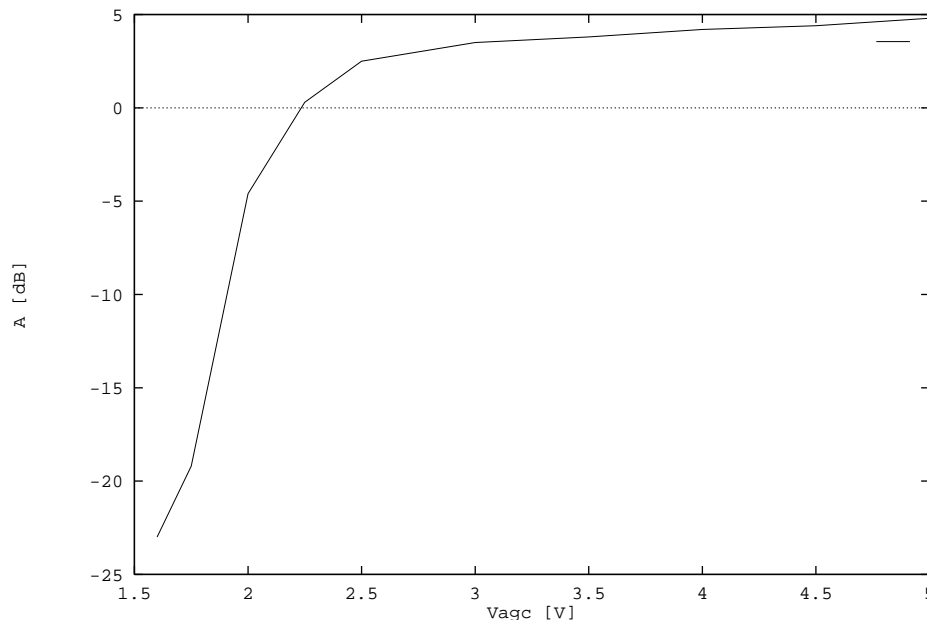


Fig.23 AGC Gain=f(Vagc)

The output 1dB compression point of the AGC circuit is 107.5dB $\mu$ V. The AGC amplifier output impedance, which must be low to drive the SAW filter, is  $56\ \Omega$ .

The SAW filter performs the channel selectivity. The SAW filter is coupled symmetrically to the input of the Mixer/oscillator (NE602). The 1.5 k $\Omega$  load resistor is intended for correct termination of the SAW filter.

The NE602 mixes the IF signal to a new centre frequency which is equal to the symbol frequency  $f_{\text{symbol}}$ . The carrier-oscillator frequency used by the mixer is  $f_{\text{IF}} + f_{\text{symbol}}$  (upper mixing). Consequently, the input spectrum will be mirrored around the centre frequency.

The carrier oscillator has a VCO constant,  $k_{\text{osc}}$ , of:

	USA	EUR
$K_{\text{osc}}$ [rad/vs]	428800	334000
range ( $\Delta U = 4.5$ v) in [kHz]	307	239

The main function of the low pass filter is removing the unwanted mixing products of the mixer. The nearest unwanted mixer components in its output spectrum are the oscillator frequency and sum component. The LPF is designed to suppress these components to 40dB under the wanted component. The measured characteristic of the LPF is shown in Fig.24.

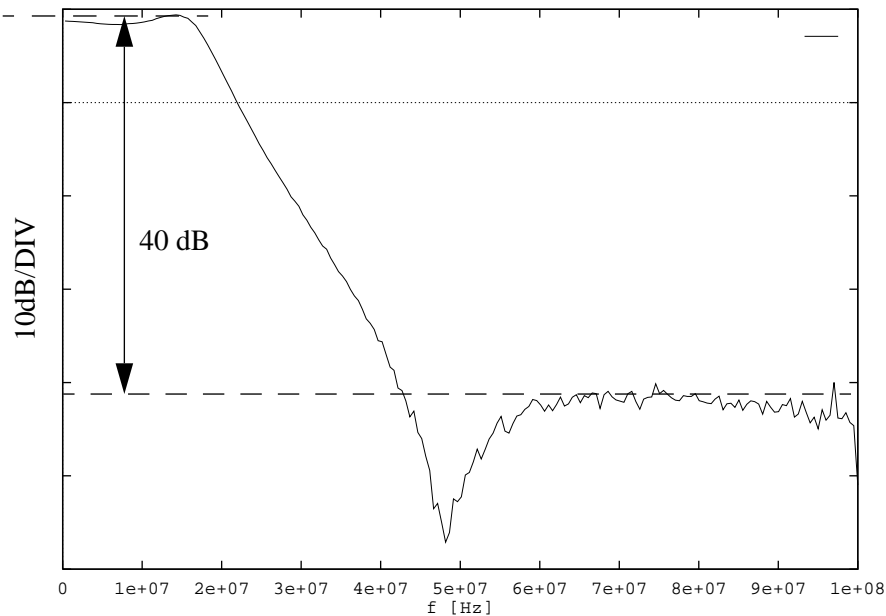


Fig.24 LPF characteristic

## 4.2 The base-band processing part

The amplifier after the low pass filter consists of two stages. The first stage, NE592, takes care of a differential amplification of 19dB. This will result in a differential output level of 111dB $\mu$ V. Because the ADC input is asymmetrical, one output pin from the NE592 is used, which is referenced to ground. The asymmetrical level at this point is 105dB $\mu$ V which is not enough according to the ADC requirements. Because the NE592 is already working at its maximum output level, a second amplifier stage is used to deliver 6.7dB extra gain. This function is performed by a single transistor (BF550).

The ADC digitizes the incoming QAM signal to 9 bits parallel words with a sample rate of  $4 \cdot f_{\text{symbol}}$ . The analog input window is 1.1V<sub>pp</sub> so the nominal input level is 111.7dB $\mu$ V

NOTE:

The TDA8761 is slightly used outside spec. With input voltage 1.1V<sub>pp</sub> and  $V_{\text{OB}}=250\text{mV}$  and  $V_{\text{OT}}=250\text{mV}$  the  $V_{\text{diff}}=1.5$  Volt which is smaller than the minimum required 1.8 Volt (see TDA8761 spec, CHARACTERISTICS).

### 4.3 The demodulator

After power up a reset should be given to the TDA8046H in order to set the internal flip-flops to a predefined position. This reset is provided on the Om5701 board with an RC combination of R32 and C30. After a high signal at the PRESET pin (which can be applied with S1) is applied, this pin is kept high long enough to reset the TDA8046H.

The measurement interface is reset with the same signal.

### 4.4 The clock oscillator

The clock oscillator runs at four times the symbol frequency used by the TDA8046. The phase is controlled by the clock recovery loop to optimize the sample moments with respect to the incoming QAM modulated signal.

The VCXO constant,  $k_{osc}$ , of the oscillator is equal to:

	USA	EUR
$k_{osc}$ [rad/vs]	4330	5025
range ( $\Delta U = 4.5$ v) in [kHz]	3.1	3.6

The clock oscillator in the OM5701 application is designed for use with a certain crystal. the crystal specifications for the VCXO are::

	USA	EUR
$f_n$ [kHz]	20000.000	27500.000
C-load [pF]	13.5	15
Mode of vibration	Fund	Fund

The same type of crystals have to be used in the VCXO to guarantee a stable operation.

### 4.5 The measurement interface

The measurement interface contains two programmable devices: a 84 pins 160 cell device and a 44 pins 32 cell device.

This solution combines high speed, provided by the 32 cell device, necessary for serial output, with a large number of logic cells available with the 160 cell device. This is necessary for implementing the control and data path processing.

The 32 cell device performs the following tasks:

- Bit clock frequency selection. This frequency is dependent on the modulation used (4, 16, 32, 64 or 256 QAM). The EPLD takes care of the divider in the PLL loop, used to regenerate the bit-clock from the symbol clock. The appropriate frequency is selected by changing the number of division.
- Parallel to serial conversion in the case the output of the TDA 8046H is in the 8-bits parallel output mode. This serial signal can be used for BER measurements with a transmission analyser.

The 160 cell device is used to take care of a number of functions:

- I2C control of all the functions implemented in the EPLDs.
- Putting the I and Q information (when the TDA 8046H is in the I/Q alternating output mode) on the two DAC's to enable monitoring these signals with a constellation analyser.
- Processing the digital information to enable functions like using GRAY coding for measurements. For this coding method the data is remapped and can be rotated.

To regenerate the bit clock from the symbol clock, a PLL is used with a minimum number of external components. Only an external divider is needed. The divider, which defines the multiplication factor, is implemented in the 32 cell EPLD. With the frequency select input (FS, 3) three VCO ranges can be selected in the PLL:

- Low: 15-30MHz
- Mid: 25-50MHz
- High: 40-80MHz

#### 4.6 Voltage levels in the IF and base-band processing parts

An overview of the peak voltage levels in the QAM demodulation section, when a QAM signal is applied to the input, is given in Fig.25.

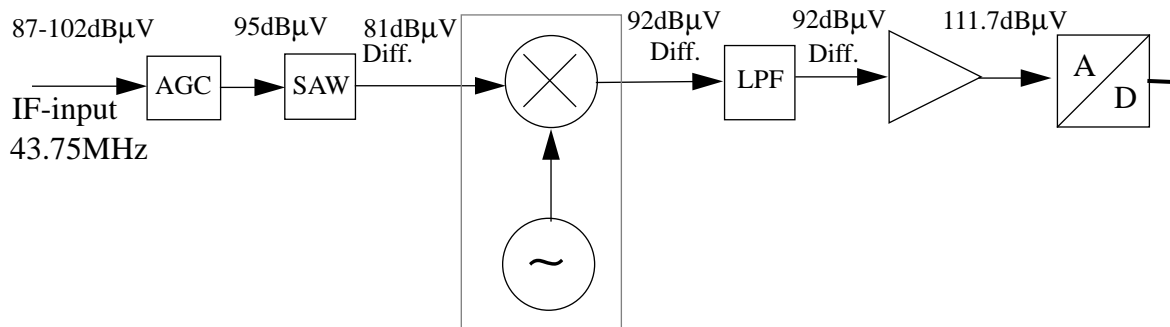


Fig.25 Power levels in the analog path

#### 4.7 Power supply of the board

The power supply can be provided by means of SMA connectors on the board, and can be divided into three parts:

- 5 Volt for the A/D converter, MECO and the peripheral parts of the TDA 8046.
- 5 Volt for the analog part of the TDA 8046, front-end and D/A converters.
- 3.3 Volt for the digital core of the TDA 8046.

#### 4.8 Decoupling measures

The TDA8046H consists of analogue blocks as well as digital blocks. To prevent distortion (especially due to switching behaviour of the digital blocks) on the sensitive parts of the TDA8046H, certain decoupling measures on the OM5701 board have been added that will reduce BER.

The clock of the TDA8046H is one of those sensitive parts. Any jitter on the rising ADC clock edges will cause phase disturbances (for example a quadrature error) in the constellation. This will translate to a higher BER. To prevent this several measures have been taken:

- The clock circuit in the TDA8046H has been decoupled. The clock circuit in the TDA uses separate supply and ground pins.
- The 3.3V core of the TDA8046H has been decoupled. The core uses two pins for power supply. The higher harmonics of the ripple on this core can cause ADC clock phase jitter. Therefore the 3.3V core pins should be decoupled. The optimal placing of the decoupling capacitors is as close as possible to pins 13 and 45. The value of the decoupling capacitors is a small value (10-22 nF) but can best be found empirically as it depends on the layout.

Another important part of the OM5701 board is the analogue part. The analogue components should be decoupled sufficiently to prevent any distortion coming from the digital supply voltage. A good method is to also split the 5V supply in an analogue and digital part as has been done on the OM5701 board.



## 4.9 Schematics

### Schematic 1 : The application board

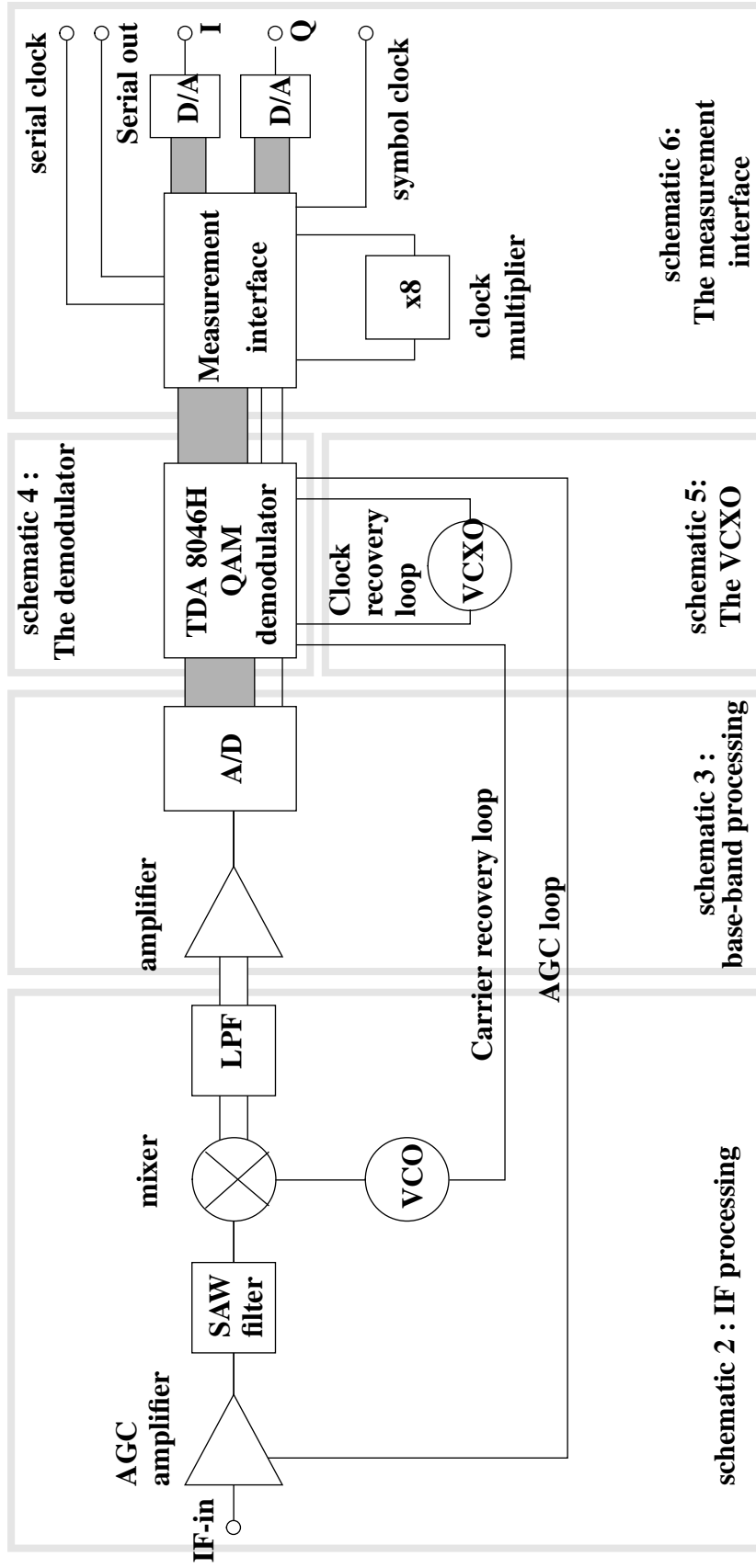


TABLE 13

component	USA	EUR
IF-freq	43.75 MHz	36.15 MHz
F <sub>s</sub>	5 MS/s	6.875 MS/s

## Schematic 2 : IF processing

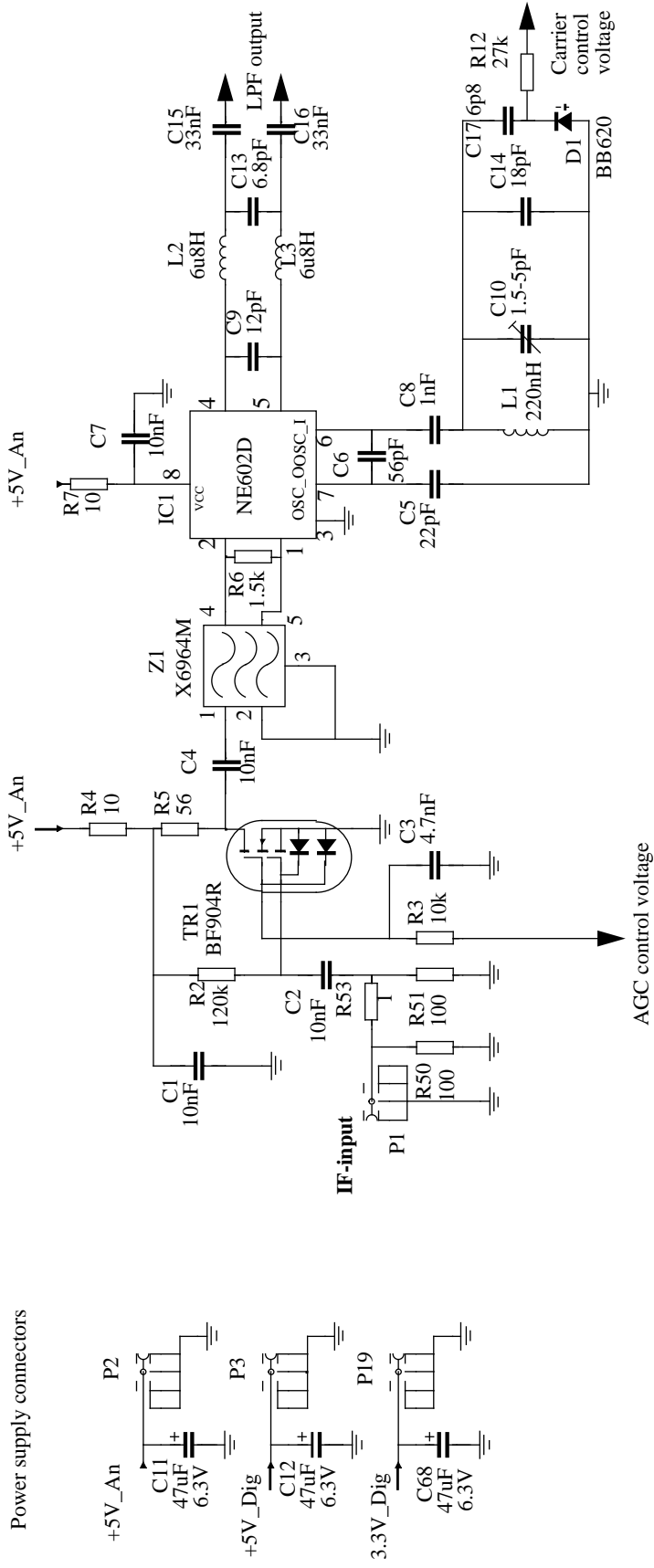
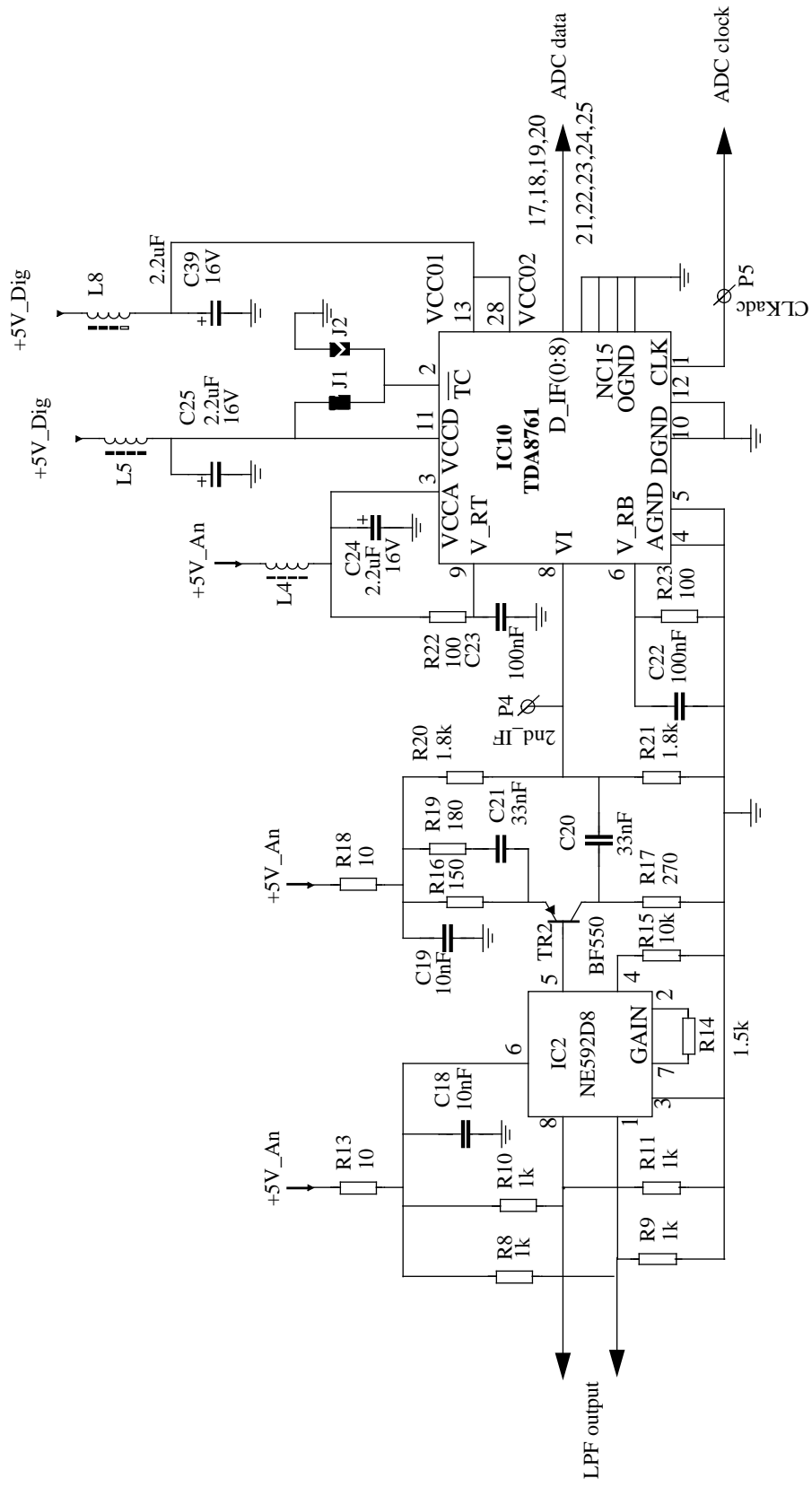


TABLE 14

component	USA	EUR
R5	56 $\Omega$	120 $\Omega$
SAW filter (Z1)	X6964M	X6966M
L1	220 nH	270 nH
C14	18 pF	22 pF

Schematic 3 : Base-band processing



### Schematic 4 :The demodulator

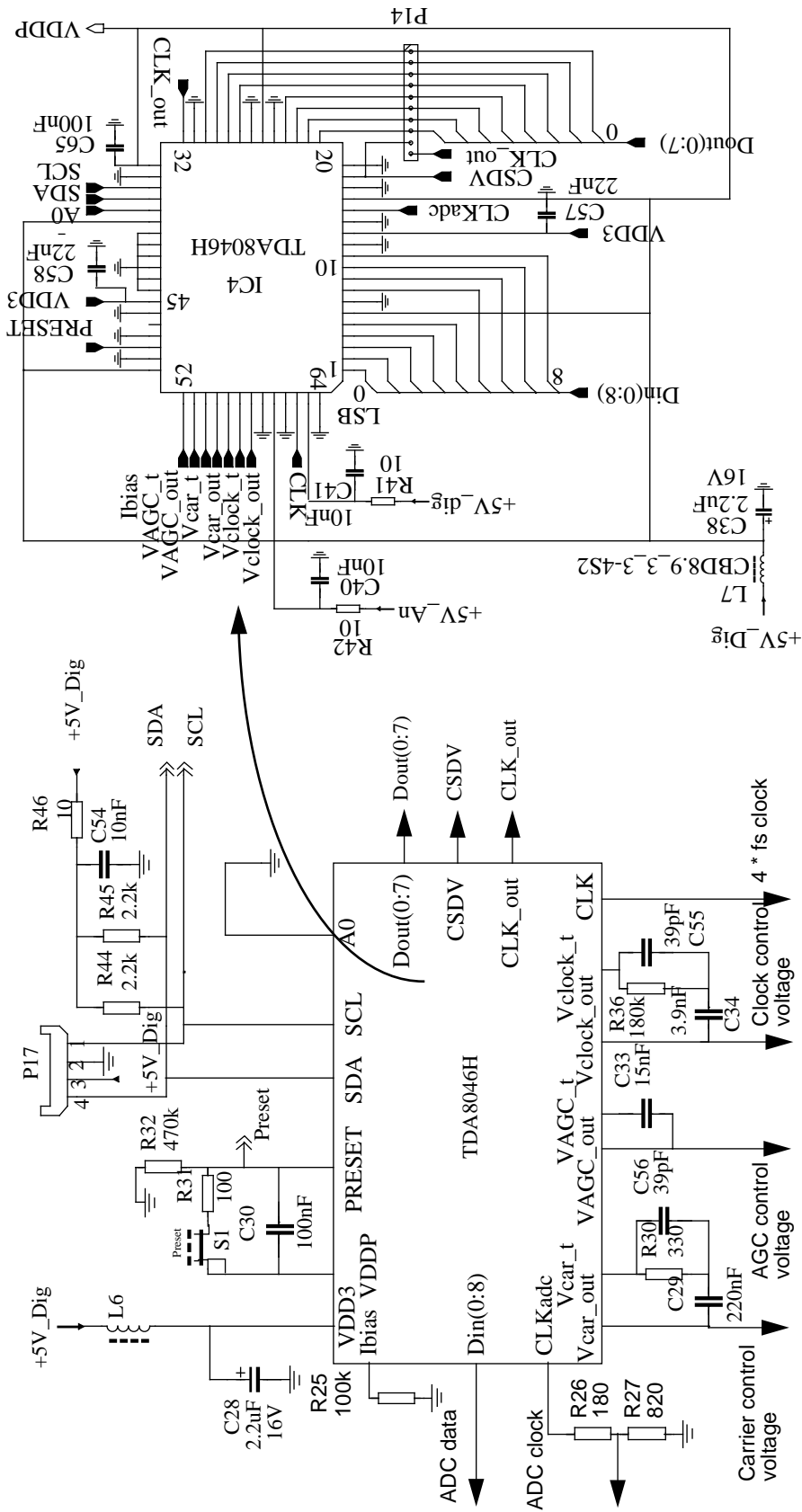


TABLE 15

component	USA	EUR
R30	330 $\Omega$	470 $\Omega$
C29	220 nF	82 nF
R36	180k $\Omega$	120 k $\Omega$
C34	3.9 nF	4.7 nF

# Schematic 5 : The VCXO

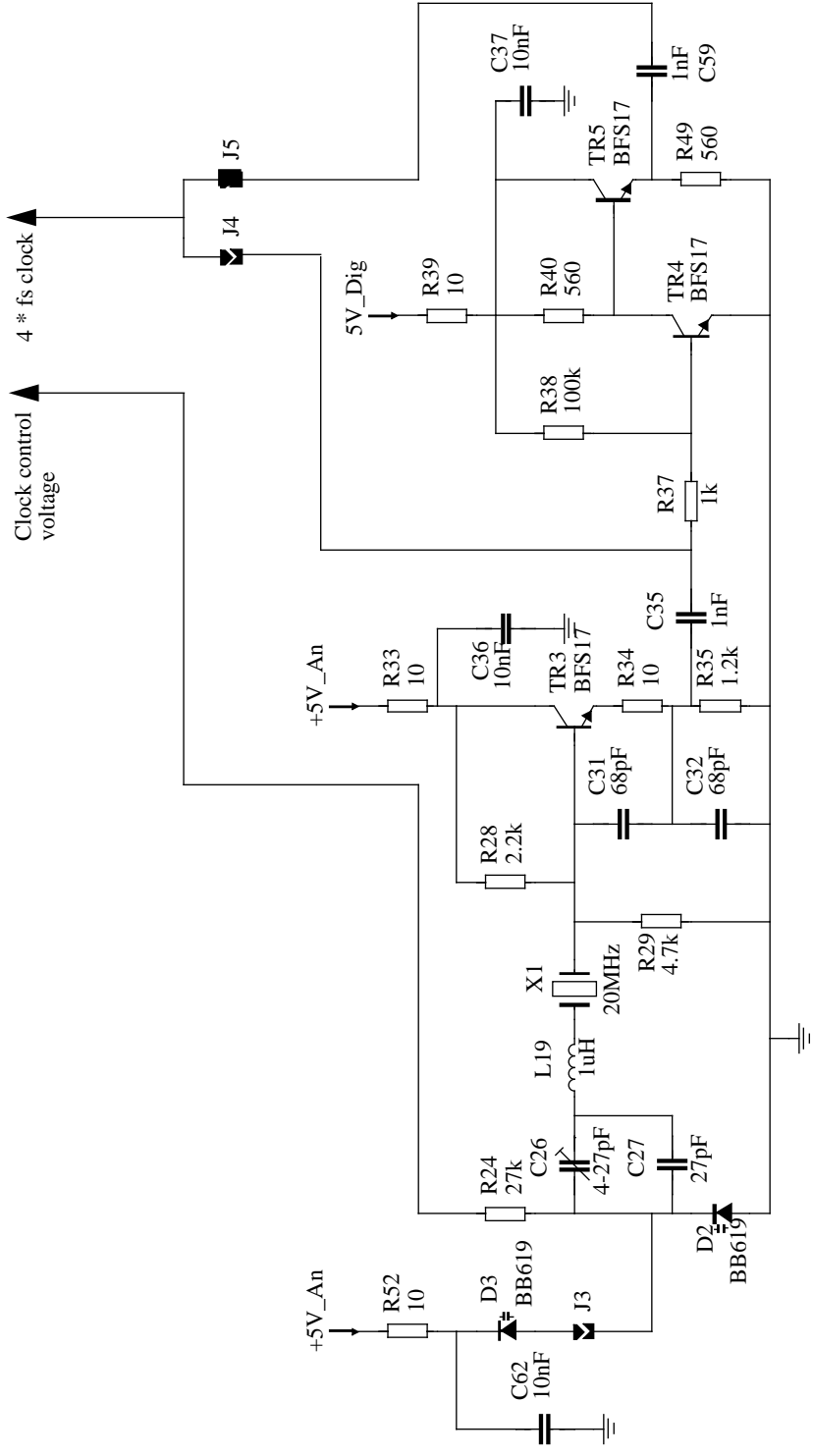
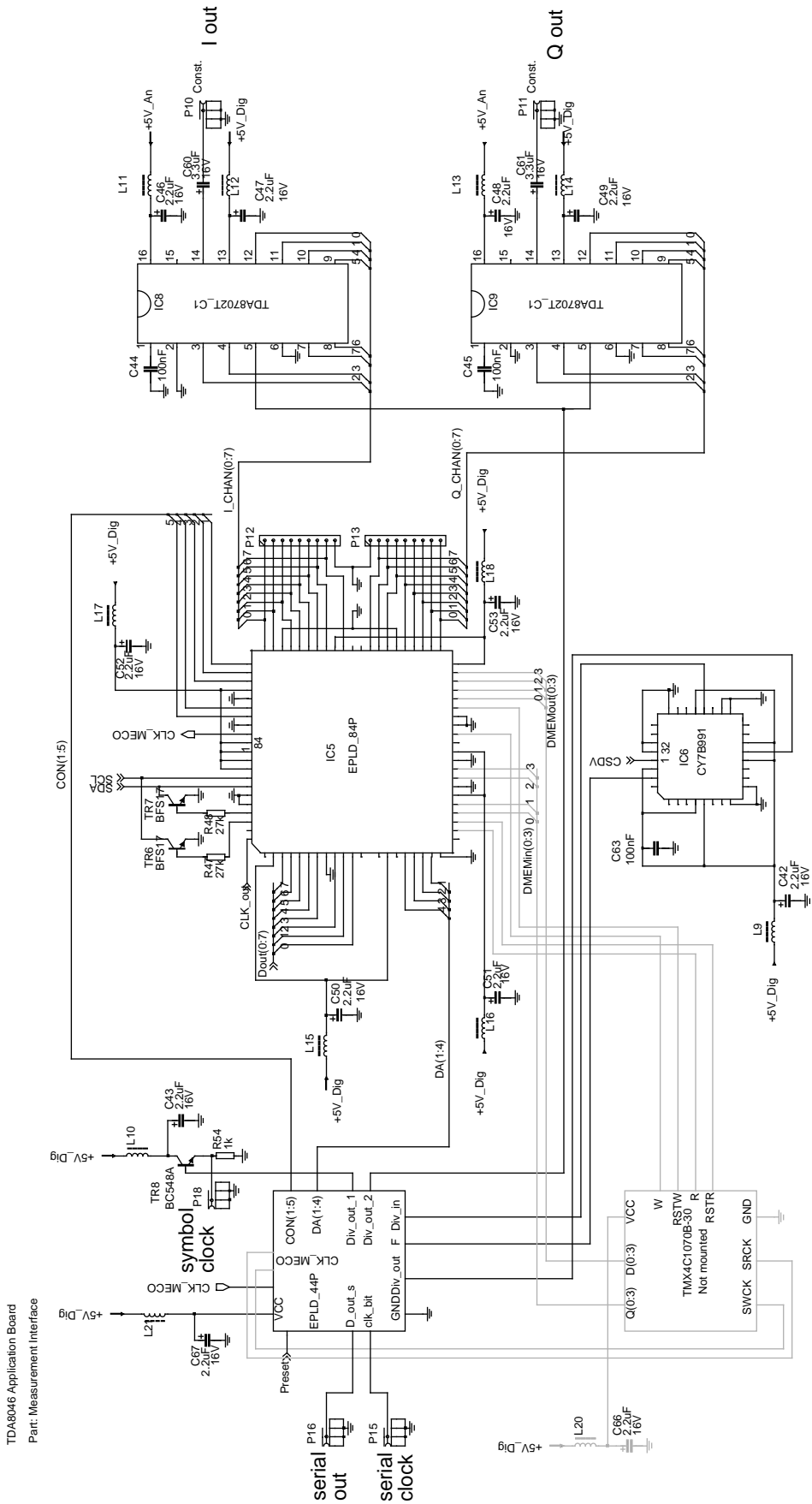


TABLE 16

component	USA	EUR
X1	20 MHz fund, C-load = 13.5 pF	27.5 MHz fund, C-load = 15 pF
C27	27 pF	removed

# Schematic 6 : The measurement interface



## 5. Measurements on the TDA 8046H application board

### 5.1 The measurement set-up

The application board consists of a QAM demodulator and MEasurement COntroller (MECO). The MECO enables an easy test interface between the QAM demodulator and measurement equipment. The board implementation is described in chapter 4. A test setup is depicted in Fig.26.

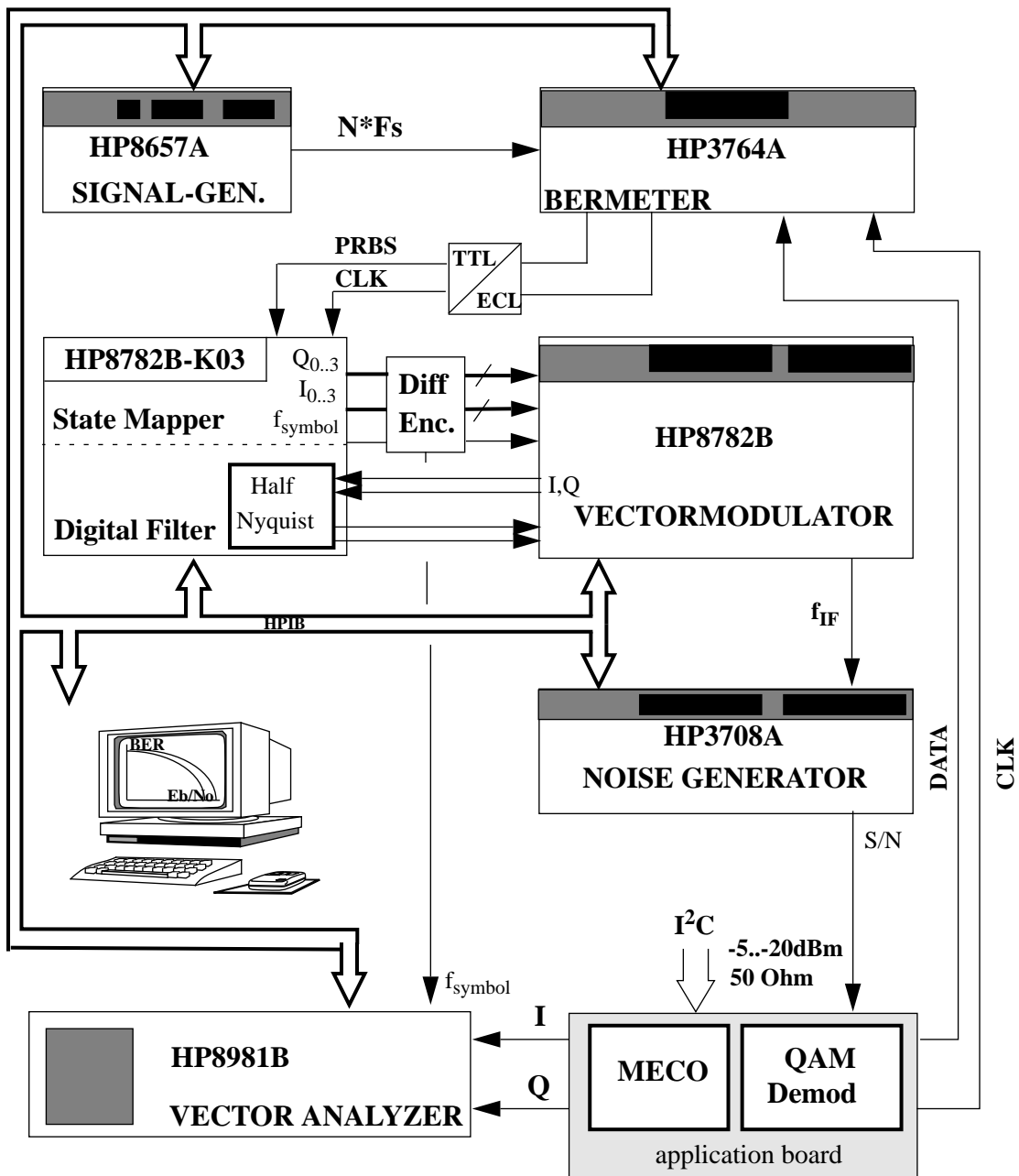


Fig.26 Test setup for BER measurement

The HP8657A generates a clock which equals the bit rate. For 256 QAM this is 8 times the symbol rate and for 64 QAM this is 6 times the symbol rate. A BER meter HP3764A generates a random bit sequence with a corresponding clock. A HP8782B-

K03 maps each 6 bits to a symbol. The 3 bits I and 3 bits Q output represent the symbol position in the constellation. I and Q are, in case of a differential encoding scheme, differentially encoded before applied to the vector analyser HP8782B.

The HP8782B generates a QAM signal at Fif, while the noise generator HP3708A adds noise. This output signal is applied to the application board. The application board is controlled by I<sup>2</sup>C.

The MEasurement CONTroller (MECO) generates two outputs. A serial data output and a bit clock which can directly be connected to the BER meter.

Also two analog outputs for I and Q are generated to show a constellation on the vector analyser HP8981B. A digital output representation on I and Q is available too in 8 bits accuracy to connect to a logic analyser or a FEC. The digital I and Q output can be straight binary or 2's complement (I<sup>2</sup>C controlled). All HP equipment is controlled by a HPIB bus and a PC.

## 5.2 Connecting the application board to the measurement setup

For correct operation, a number of points in the measurement setup must be checked first:

### QAM generator

- Adjust the symbol rate of generator the to (for example) 5 Msymbols/s. Note that for different modulation schemes different bit rates must be used to obtain this symbol rate.
- Set the RF frequency to 43.75 MHz for USA or 36.15 MHz for EUR.
- Adjust the RF level at the QAM demodulator IF-input (50Ω) to a value between 93dBμV and 127dBμV

### Constellation analyser

- Connect the two 75Ω DAC outputs (Marked "to constellation analyser") from the demo board to the analyser.

### Transmission analyser

- To make BER measurements connect the bit clock (CLK-bit) and the serial data stream (D-out serial) to the transmission analyser.

### Demo board

- Plug an I<sup>2</sup>C-interface board into the parallel port of a PC. Connect the I<sup>2</sup>C bus from the interface board to the demo board.
- Apply power to the board. The digital- (+5V-D) and analog (+5V-A) supply can be supplied separated if necessary.
- start the program DVB2.EXE to control this board

### IF Input

- The RF QAM signal must be applied on this point. The input level must be between 93dBμV and 127dBμV for correct operation. The input impedance is 50Ω.

### Demodulated data/Bit-clock output

- The serial demodulated data, together with the bit-clock, can be used for BER measurements. The bit rate is depending on the used constellation and symbol rate.

### Constellation outputs

- The outputs can be directly connected to an constellation analyser. The output impedance is 75Ω. It is not possible to measure an eye-pattern at one of the outputs. The cause of this restriction is the 5MHz sample rate of the I and Q signals, which is not high enough to prevent aliasing at the outputs. That is why the 3MHz wide base band signals, I and Q, can't be recovered by filtering. For this reason the DAC outputs are not filtered and consequently the outputs change step wise. Each level represents the I and Q value, used by the TDA8046 to retrieve the symbols. When these signals are supplied to the constellation analyser a correct constellation diagram will be shown.

### I<sup>2</sup>C

- The TDA8045 and the EPLD are controllable via I<sup>2</sup>C. For this purpose a PC program, called DVB2, is available to make adjustments and read out data in a convenient way.



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### **CSDV output**

- The TDA 8046 board is provided with a  $50\Omega$  output where the symbol frequency can be adapted. When the demodulator is locked to the QAM signal DVB will give the message "lock: yes". A constellation diagram can be seen when you enter the test mode by clicking on "<CONSTELLATION>". To measure the Bit Error Rate you must switch back to the mode "<MEASUREMENT>". Be sure that the I-axis is inverted because of a mirrored spectrum after mixing down. When the mapping is not differentially (for example GRAY coding), the phase ambiguity of 90 degrees can be adjusted by rotating the constellation by clicking "<rotate>" in the MECO menu. When no noise is added the BER must be zero. Rotate the constellation until this BER is displayed. Now, the BER measurement is possible

### 5.3 BER measurement with Differential (DVB) coding

The performance of the demodulator design is ultimately translated in a number for the errors after demodulation; the BER. The HP8782B-K03 generates according scheme 1 or 3 in one quadrant (4 LSB's). The 2 MSB's are differentially encoded in a separate module. After QAM modulation, after the channel the TDA8046H performs the QAM demodulation, decoding according scheme 1 or 3 which includes differential decoding on the 2 MSB's. It is important that the MECO is transparent, which is achieved when scheme 1 or 3 is chosen (by I<sup>2</sup>C) and NO rotation. (see Fig.27). Note that the MECO does NOT support 32 QAM mode. A special MECO is required.

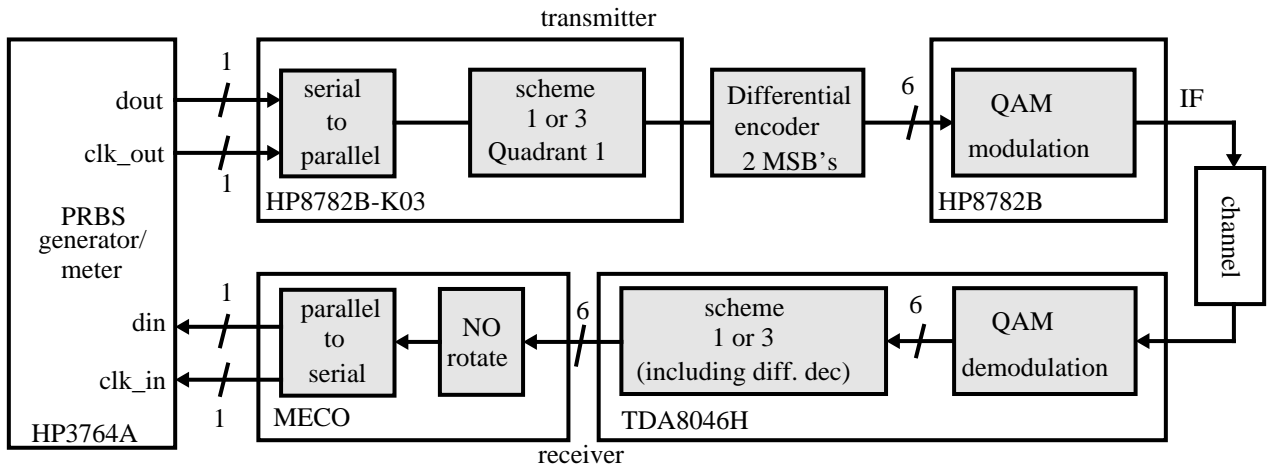


Fig.27 BER measurement with differential coding

With the BER measurement done at different  $E_b/N_0$  values, a graphic like the one in Fig.28 is obtained.

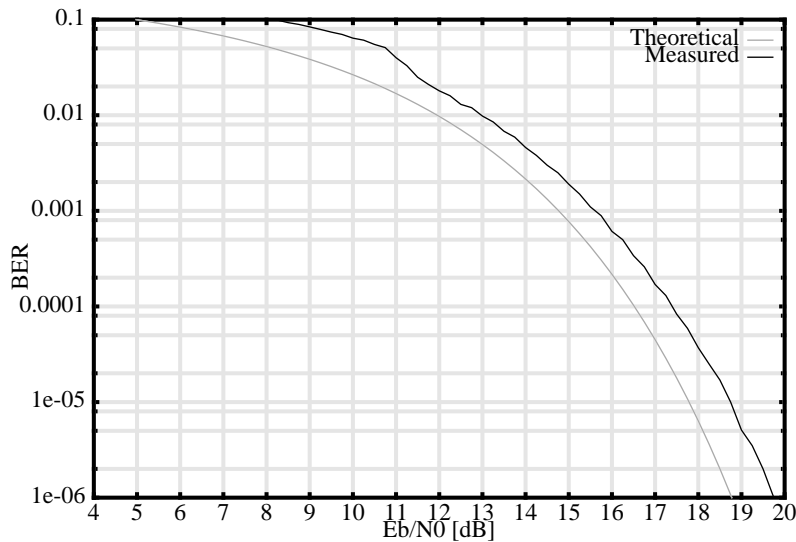


Fig.28 AWGN BER measurement for 64 QAM using differential coding

From this graphic the IL can be derived as is explained in chapter 1.2.

### 5.4 BER measurement with Gray coding

In this chapter a method is described to do this without the necessity of the differential encoder from Fig.26, namely GRAY coding.

Fig.29 shows the test setup. The bit sequence generated by the PRBS generator is serial to parallel converted and Gray encoded in HP8782B\_K03. The Gray encoding schemes are shown in APPENDIX C. The HP8782B performs the QAM modulation according scheme 4 of the TDA8046H.

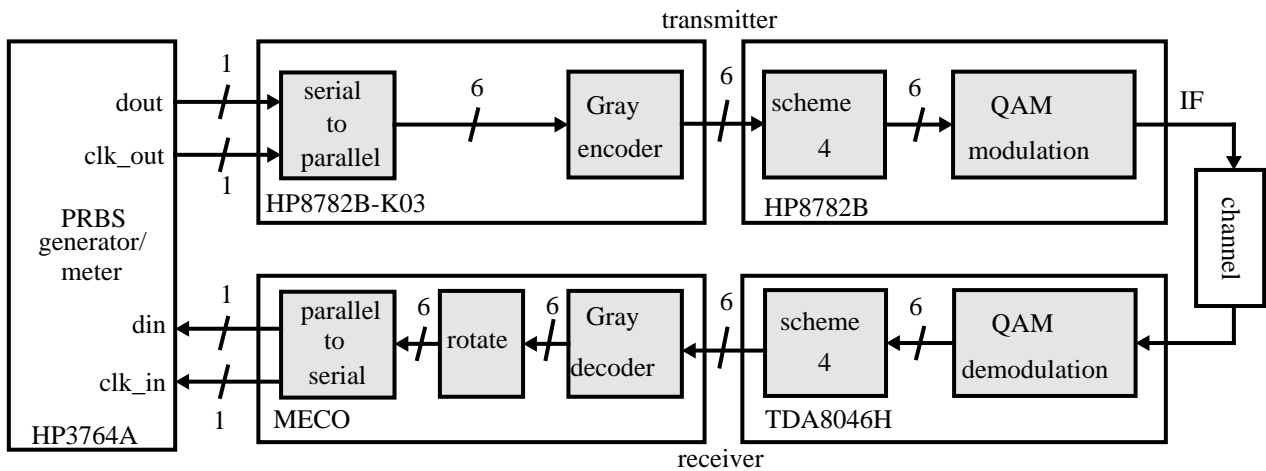


Fig.29 BER measurement with Gray code

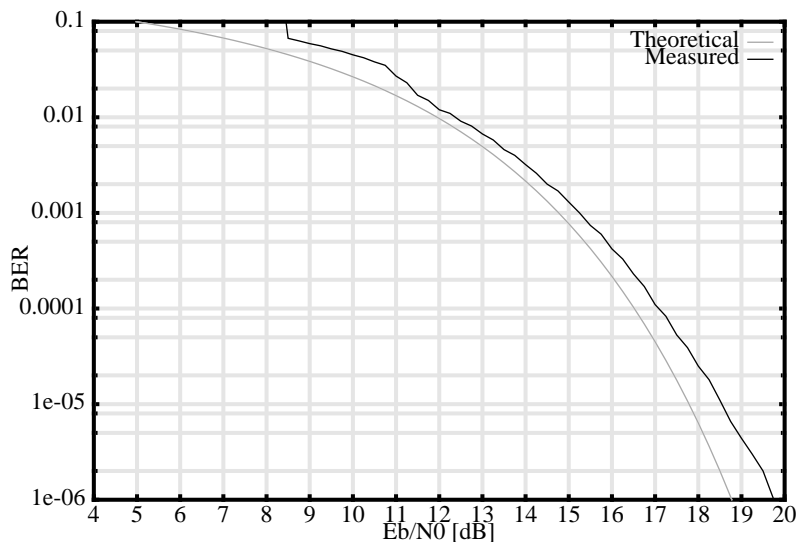


Fig.30 AWGN BER measurement for 64 QAM using Gray coding

On the receiver side, the TDA8046H performs the QAM demodulation according scheme 4. The MECO performs the Gray decoding. A rotator turns the constellation in multiples of 90 degrees. By controlling this rotator by I<sup>2</sup>C the phase ambiguity of 90 degrees can be compensated. In case the frequency spectrum is swapped, the demodulation in the TDA8046H must be done by toggling sign of the sine demodulation function. Note that there is a relation between the sign of the sine and the

---

sign of the phase detector. Toggling the first implies toggling the second. A parallel to serial convertor in the MECO finally generates a serial data stream and clock which is fed to the HP3764A BER meter which gives the performance of the system.

Note that no 100% Gray code is possible for a 32QAM scheme! This means that comparing the measured 32QAM BER curve with the theoretical one will give an implementation loss which is slightly too high. This is caused by 8 neighbouring symbols at the right and left hand side which have Hamming distance 2 in stead of one. A precise comparison can be achieved by redefining the BER curve. This is not described in this application note.

## APPENDIX A Transmitter Half Nyquist Filter

Table 17: contains a 20% transmitter Half Nyquist filter, which perfectly matches to the TDA8046H 20% receiver filter.

The total length: 63 taps

Non-zero CSD bits: 183

Average Passband Gain: 6150

DC gain: 6143

Peak to Average Ratio (PAVR): 1.76!

**Table 17: 20% Half Nyquist transmitter filter coefficients**

Poly phase components of Half Nyquist filter.					
Poly phase component 2.0			Poly phase component 2.1		
Coefficient	Value	CSD	Coefficient	Value	CSD
$h_t(1), h_t(-1)$	1430	10T0T010T0T0	$h_t(0)$	1607	10T00100100T
$h_t(3), h_t(-3)$	403	10T001010T	$h_t(2), h_t(-2)$	969	1000T001001
$h_t(5), h_t(-5)$	-306	T0T0100T0	$h_t(4), h_t(-4)$	-67	T000T01
$h_t(7), h_t(-7)$	-130	T00000T0	$h_t(6), h_t(-6)$	-298	T00T0T0T0
$h_t(9), h_t(-9)$	167	1010100T	$h_t(8), h_t(-8)$	61	1000T01
$h_t(11), h_t(-11)$	53	10T0101	$h_t(10), h_t(-10)$	151	1010T00T
$h_t(13), h_t(-13)$	-103	T010T001	$h_t(12), h_t(-12)$	-52	T010T00
$h_t(15), h_t(-15)$	-19	T0T01	$h_t(14), h_t(-14)$	-83	T0T0T01
$h_t(17), h_t(-17)$	64	1000000	$h_t(16), h_t(-16)$	41	101001
$h_t(19), h_t(-19)$	2	10	$h_t(18), h_t(-18)$	44	10T0T00
$h_t(21), h_t(-21)$	-37	T00T0T	$h_t(20), h_t(-20)$	-30	T00010
$h_t(23), h_t(-23)$	5	101	$h_t(22), h_t(-22)$	-20	T0T00
$h_t(25), h_t(-25)$	20	10100	$h_t(24), h_t(-24)$	21	10101
$h_t(27), h_t(-27)$	-6	T010	$h_t(26), h_t(-26)$	7	100T
$h_t(29), h_t(-29)$	-9	T00T	$h_t(28), h_t(-28)$	-12	T0100
$h_t(31), h_t(-31)$	4	100	$h_t(30), h_t(-30)$	-2	T0

The coefficients are listed in Canonical Signed Digit (CSD) notation. T represents the value -1. The CSD notation describes a very compact implementation  $h_t(26), h_t(-26)$  using CSD: value=7; CSD=100T

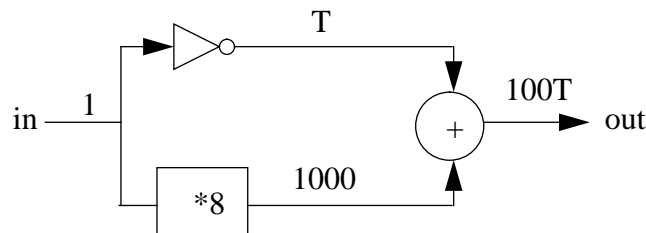


Fig.31 Implementation example of CSD=100T

## APPENDIX B Theoretical BER/SER curve

The received signal contains the transmitted symbols and noise. Due to noise, a transmitted symbol can be received in a neighbouring decision area and as a consequence a wrong decision will be made. When  $\sqrt{E_o}$  is the energy of the signal and  $\sigma^2=N_o/2$  is the variance of the white Gaussian noise, the probability density function is depicted in Fig.32. The probability of error  $P_e$  is given by the dashed area and is described by the  $Q(\sqrt{E_o}/\sigma)$  function [HAY; pp. 318-322].

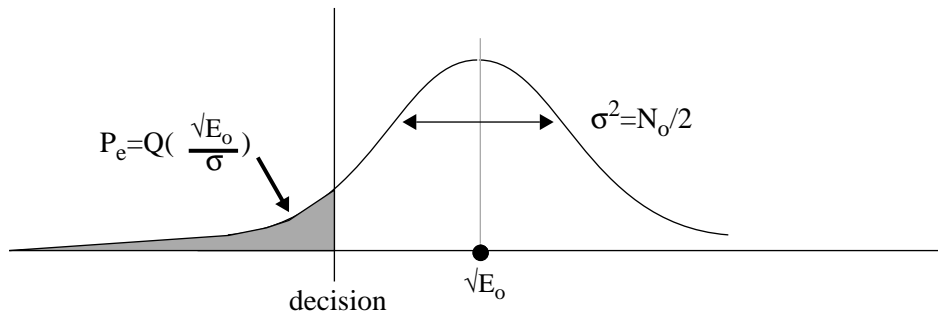


Fig.32 Probability of error and the Q() function

In case of 64 QAM, there are 8 possible symbol location on the I and Q axes. The probability density function of the I or Q axis is depicted in Fig.33

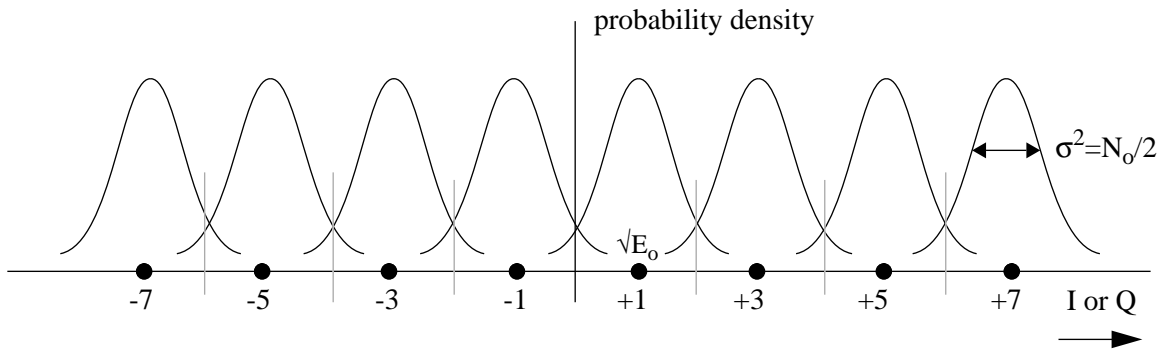


Fig.33 Probability density function of I or Q axis for 64 QAM.

The probability of error for the symbols -7 and +7 equals

$$P_e'(\text{border}) = Q\left(\frac{\sqrt{E_o}}{\sigma}\right) = Q\left(\sqrt{\frac{2E_o}{N_o}}\right) \quad (23)$$

For the symbols -5,-3,-1,+1,+3,+5 the probability of error equals

$$P_e'(\text{middle}) = 2Q\left(\frac{\sqrt{E_o}}{\sigma}\right) = 2Q\left(\sqrt{\frac{2E_o}{N_o}}\right) \quad (24)$$

For M-ary QAM, this probability of error for one dimension  $P_e'$ , when supposing each symbol has the same probability of occurrence  $p=1/\sqrt{M}$ , can generally be written as

$$P_e' = p \left( 2P_e'(\text{border}) + (\sqrt{M} - 2)P_e'(\text{middle}) \right) = 2 \left( 1 - \frac{1}{\sqrt{M}} \right) Q \sqrt{\frac{2E_o}{N_o}} \quad (25)$$

Since the in-phase and quadrature components of M-ary QAM are independent, the probability of correct reception of a symbol is given by

$$P_c = (1 - P_e')^2 \quad (26)$$

The probability of symbol error (SER) for M-ary QAM is given by

$$\text{SER} = 1 - P_c = 1 - (1 - P_e')^2 \approx 2P_e' = 4 \left( 1 - \frac{1}{\sqrt{M}} \right) Q \left( \sqrt{\frac{2E_o}{N_o}} \right) \quad (27)$$

To calculate the probability of symbol error for M-ary QAM, it is more convenient to express it in the symbol energy (average energy)  $E_s$ , i.e.:

$$E_s = \frac{2(M-1)}{3} E_o \quad (28)$$

where M is the number of constellation points (e.g. M=4, 16, 32, 64).

It is obvious that the energy per bit  $E_b$  equals

$$E_b = \frac{E_s}{\log_2 M} \quad (29)$$

With the help of equations (1.6) to (1.8) the probability of symbol error can also be expressed as

$$\text{SER} = 4 \left( 1 - \frac{1}{\sqrt{M}} \right) Q \left( \sqrt{\frac{3}{M-1} \frac{E_s}{N_o}} \right) = 4 \left( 1 - \frac{1}{\sqrt{M}} \right) Q \left( \sqrt{\frac{3 \log_2 M E_b}{M-1} \frac{1}{N_o}} \right) \quad (30)$$

$E_s$  is the symbol energy in each interval  $T_s$ , where  $T_s$  is the symbol duration. The signal power  $P_s$  is the symbol energy per time interval, i.e.

$$P_s = \frac{E_s}{T_s} \quad (31)$$

The noise power  $P_N$  is the total noise power in the Nyquist band. When  $N_o$  is the noise power per Herz and  $f_s$  is the noise equivalent band width of the half Nyquist receiver filter, the total noise power equals

$$P_N = N_o f_s = \frac{N_o}{T_s} \tag{32}$$

The ratio  $P_S/P_N$  will be written as  $S/N$ . The relation between  $(E_b/N_o)$  and  $(S/N)$  can easily be obtained by combining equations (1.8), (1.10) and (1.11) which gives

$$\frac{E_b}{N_o} = \frac{1}{\log_2 M} \frac{S}{N} \tag{33}$$

Furthermore, since each symbol now conveys  $\log_2 M$  bits, and with Gray encoding and low SER values, each symbol error causes one bit error, the Bit Error Rate equals

$$BER = \frac{SER}{\log_2 M} \tag{34}$$

The symbol and bit error rate formulas as function of  $E_b/N_o$  or  $S/N$  can be obtained by combining the equations (30), (33) and (34) are given in TABLE 18.

**TABLE 18 Error rate functions (M is the number of constellations points)**

Coding	parameter	ERROR RATE	
		Symbol Error Rate (SER)	Bit Error Rate (BER)
Gray code	$E_b/N_o$	$4\left(1 - \frac{1}{\sqrt{M}}\right)Q\left(\sqrt{\frac{3\log_2 M E_b}{(M-1)N_o}}\right)$	$\frac{4}{\log_2 M}\left(1 - \frac{1}{\sqrt{M}}\right)Q\left(\sqrt{\frac{3\log_2 M E_b}{(M-1)N_o}}\right)$
	$S/N = E_s/N_o$	$4\left(1 - \frac{1}{\sqrt{M}}\right)Q\left(\sqrt{\frac{3}{(M-1)}\frac{S}{N}}\right)$	$\frac{4}{\log_2 M}\left(1 - \frac{1}{\sqrt{M}}\right)Q\left(\sqrt{\frac{3}{(M-1)}\frac{S}{N}}\right)$



The curves from table 1 are depicted in Fig.34.

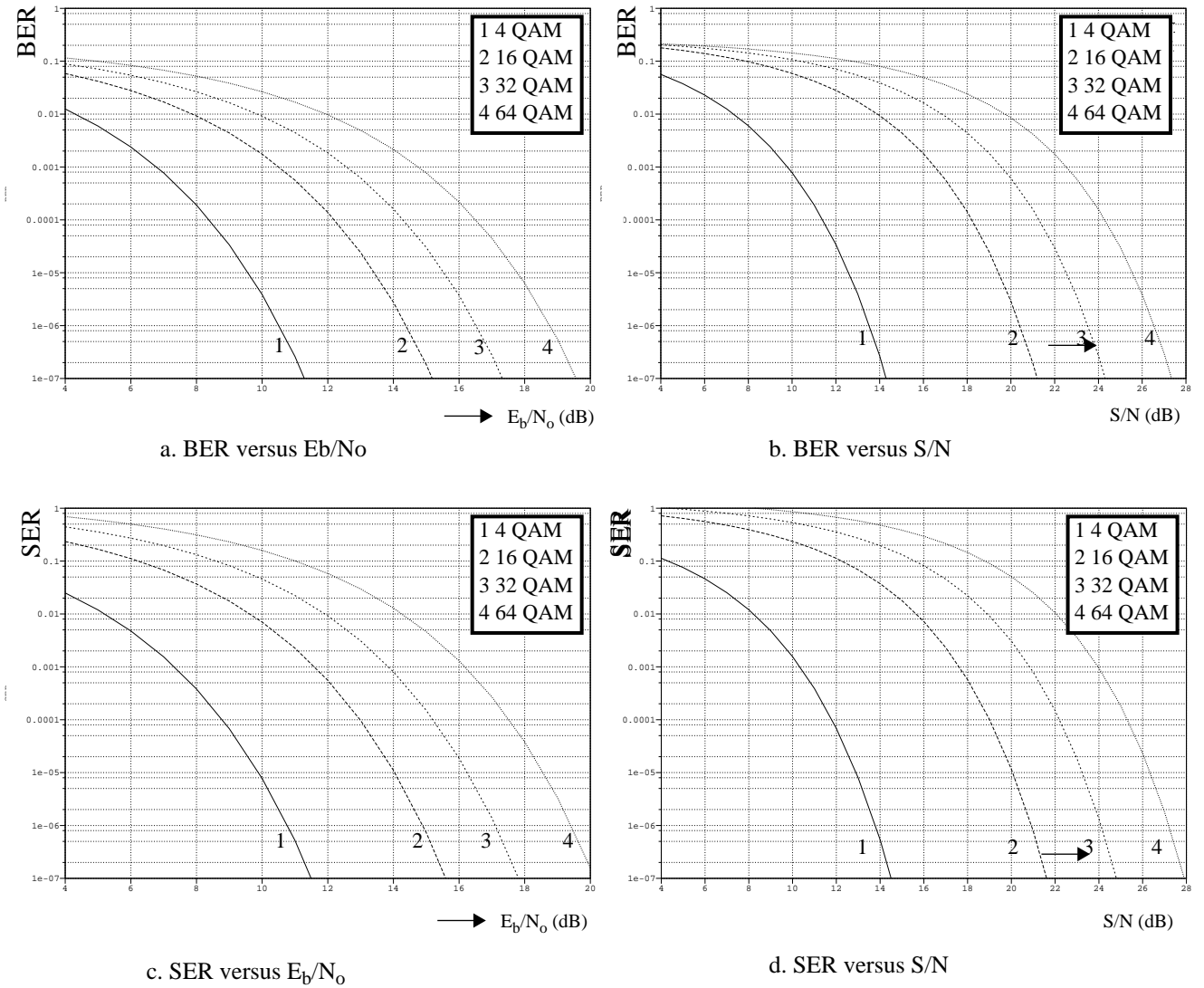
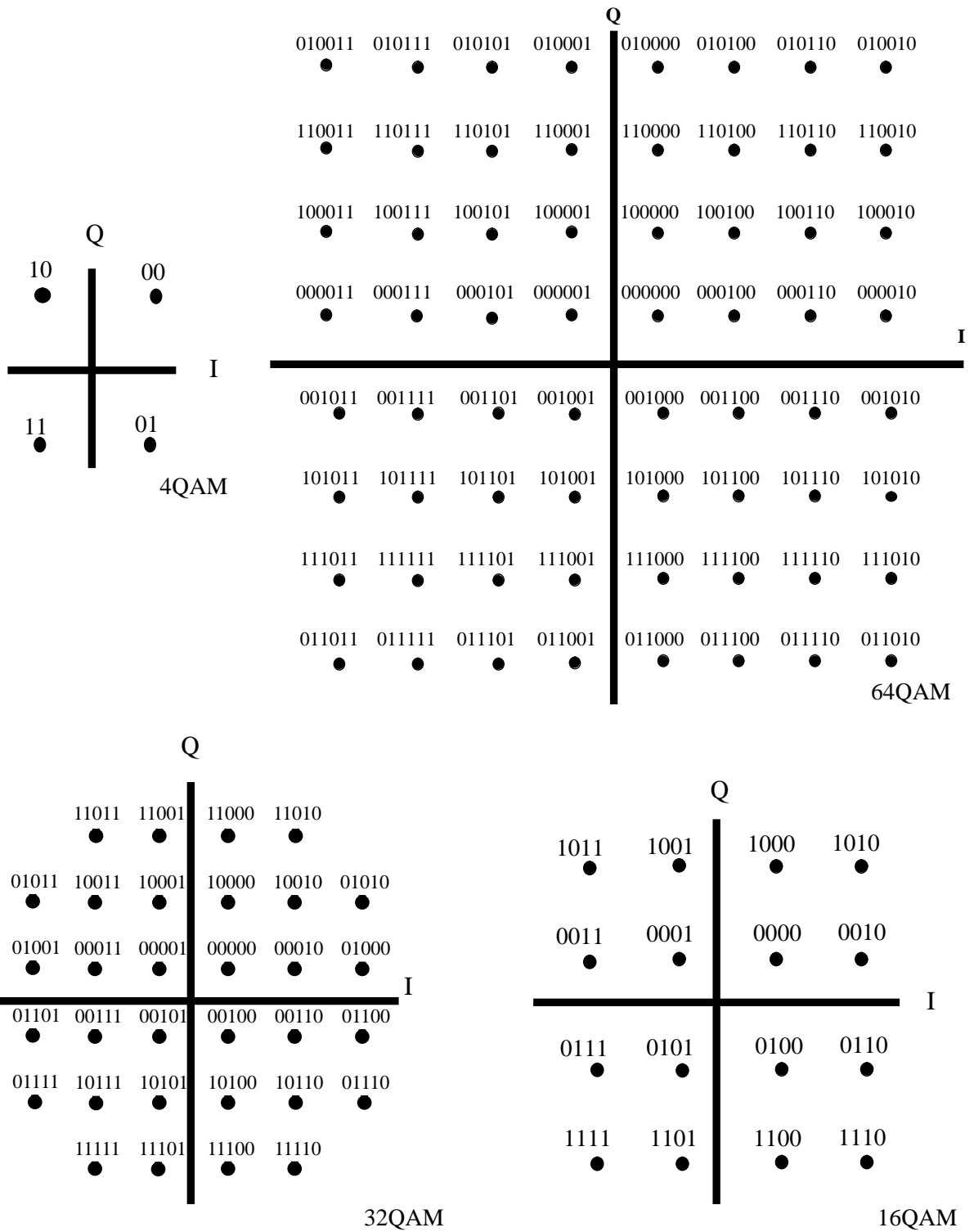
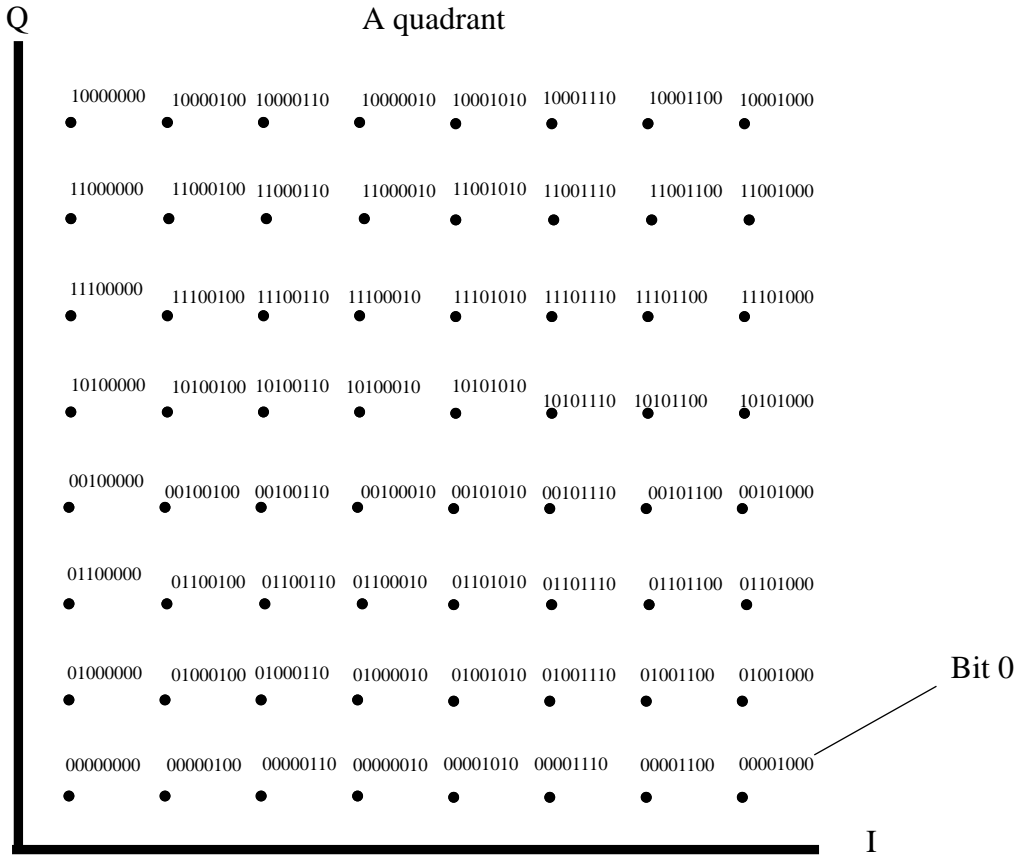


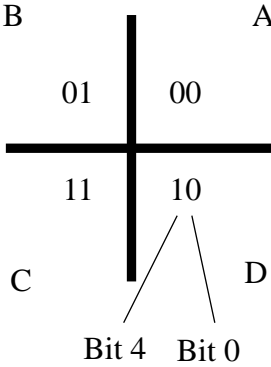
Fig.34 QAM curves for different constellations

## APPENDIX C Gray coding schemes





Gray coding for 256 QAM (quadrant A)



Values for bit positions 0 and 4 for quadrants A to D

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## APPENDIX D Relation between Eb/N0 and S/N

$$\frac{S}{N} = \frac{E_b \cdot f_B}{N_0 \cdot B_N} = 2^{\log(M)} \frac{E_b}{N_0} \quad (35)$$

Where M represents the number of constellation points e.g. 256,64, etc.

$$\frac{S}{N}_{(dB)} = \frac{E_b}{N_0}_{(dB)} + 10 \cdot \log\left(2^{\log(M)}\right) \quad (36)$$

For the most common QAM modes the values are given in table TABLE 19

**TABLE 19**

M	$10 \cdot \log\left(2^{\log(M)}\right)$
256	9.03 dB
64	7.78 dB
32	7 dB
16	6.02 dB
4	3 dB